Rensselaer Polytechnic Institute

Computer Hardware Design – ECSE 4770

Lab Assignment 1 - Observing Transmission Line Effects
Rev. F

Objective

- To exhibit the problems associated with driving computer busses by examining the reflections in a 50-ohm coaxial transmission line.

Background Information

The [Keysight Digital oscilloscope (model DSOX6004A](#)) is a modern oscilloscope with its own embedded computer and has a graphical user interface. The oscilloscope has four channels, at 1GHz of bandwidth. The passive probe (N2894-60002) has a bandwith of 700MHz, a 10M ohm impedance.

Related Web addresses

Motorola
- Main site: http://www.mot.com/

Texas Instruments
- Main site: http://www.ti.com
- Digital logic data sheets: http://www.ti.com/sc/docs/products/logic/

Tektronix
- XYZ's of Oscilloscopes: http://www.tek.com/Measurement/App_Notes/XYZs/03W_8605_2.pdf

Procedure

General Instructions: Careful wiring is imperative in this lab since the 74S05 typically generates rise times in the 2-nanosecond range. Position the 74S05 as close as possible to one of the BNC connectors into which the 50-ohm cable will be plugged. The ground for the oscilloscope probe must be no more than a couple of inches long and should be connected directly to the ground pin of the I.C. package under observation. It is

also advisable to install bypass capacitors (0.1uF) between the +5 V and GND pins of each I.C. to ensure clear signals.

Note that for the report, "observe" implies including the scope output and/or measured data.

Part 1

Set up your oscilloscope.

    a) Build the circuit shown in Figure 5 on the proto-board. Follow the suggestions made above. You will need to select a value for the capacitor C1, using the data sheet for the 555 timer. The output signal should be a relatively low noise periodic signal that can be used to study the different scope modes. You need not worry about the value or placement of R for this part. Attach the probe to the output (pin 3) of the 555 timer.

    b) Obtain and observe a stable trace of the 555. Try using the "runt" triggering modes. Try the horizontal delay mode. Describe the effects these modes have.

    c) Change the capacitor on pins 2/6. How does this affect the output?

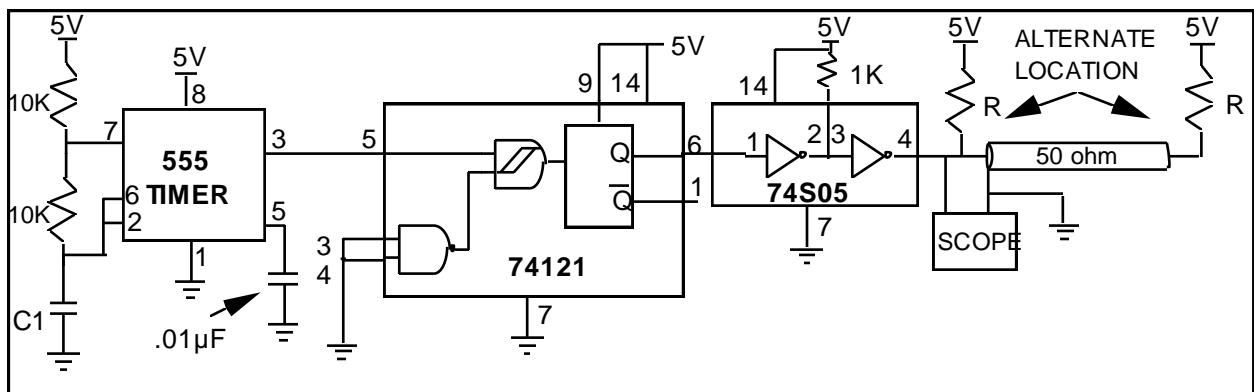   d) Observe the effect of changing one of the 10-Kohm resistors.

Figure 1: Wiring diagram for Part 1

Part 2

Move the scope probe to the output of the 74S05 just in front of the coax cable. The 74S05 open collector Schottky gate has 20 mA sinking capability.

    a) It will not be possible to correctly drive the 50-ohm impedance cable with this gate. Why is this? Refer to the data sheet for the 74S05.

    b) Use a 1 Kohm resistor for R and place it at the end of the 50-ohm cable. Observe line reflections and show how to measure the velocity of propagation in the cable using those reflections. Show your calculations and record your result.

    c) Repeat b) with R relocated at the 74S05 output.

    d) Repeat b) with additional lengths of cable.

    e) Why does the leading edge of the pulse look different from the falling edge?

    f) What is the smallest safe value of R? What criteria determine this value?

g) Use the criteria you found in f) to redesign the termination to have a pull-up and pull-down resistor, R1 and R2. Match to the minimum safe value of R. Repeat b) with this new termination.

Part 3

The 74128 50-ohm cable driver is a TTL chip designed expressly for driving 50-ohm cable. Rebuild the circuit using the 74128 instead of the 74S05.
   a) Observe any reflections now on the cable.
   b) Recalculate the minimum safe R. Refer to the data sheet for the 72128 and note that the 74128 can sink 48 mA.
   c) Adjust R to minimize line reflection.

Part 4

Try any of the other drivers or receivers whose data sheets are enclosed. Use a tri-state driver, like the 74ls241. Observe the signals on the line when there is no terminator (this is common on small computer busses). Some additional things to try are:
   a) Add pull-up resistors in the middle of the cable using T connectors. Describe their effect on the signal.
   b) Drive the line with multiple open collector gates. Think about how the circuit for a bus like this would look, and explain how it works.
   c) Try plugging the end of the 50-ohm cable directly into the scope input and observe the signal at the end of the line.

Part 5

Try assembling a 7474 Edge Triggered flip-flop out of individual gates, as shown in Figure 2 (using the 7400, 7410, or 7420 as building blocks).
   a) Observe the edge triggering and give a verbal explanation of its behavior.
   b) Attempt to excite a race by driving both the data and clock inputs simultaneously (i.e. drive both inputs with the same signal).
   c) Try introducing some small parasitic capacitance on various gate outputs to influence the outcome.
   d) Try using 74S parts.

Table 1: Typical characteristics of SN54 and SN74 series flip-flops

	TYPICAL CHARACTERISTICS		DATA TIMES		TEMPERATURE RANGE	
DWG REF	Fmax (MHz)	Pwr/F-F (mW)	Setup(ns)	Hold(ns)	55 C - 125 C	0 C - 70 C
Q	110	75	3	2	SN54S74	SN74S74
	43	75	15	5	SN54H74	SN74H74
	33	10	25	5	SN54LS74	SN74LS74
	25	43	20	5	SN5474	SN7474
	3	4	50	0	SN54L74	SN74L74
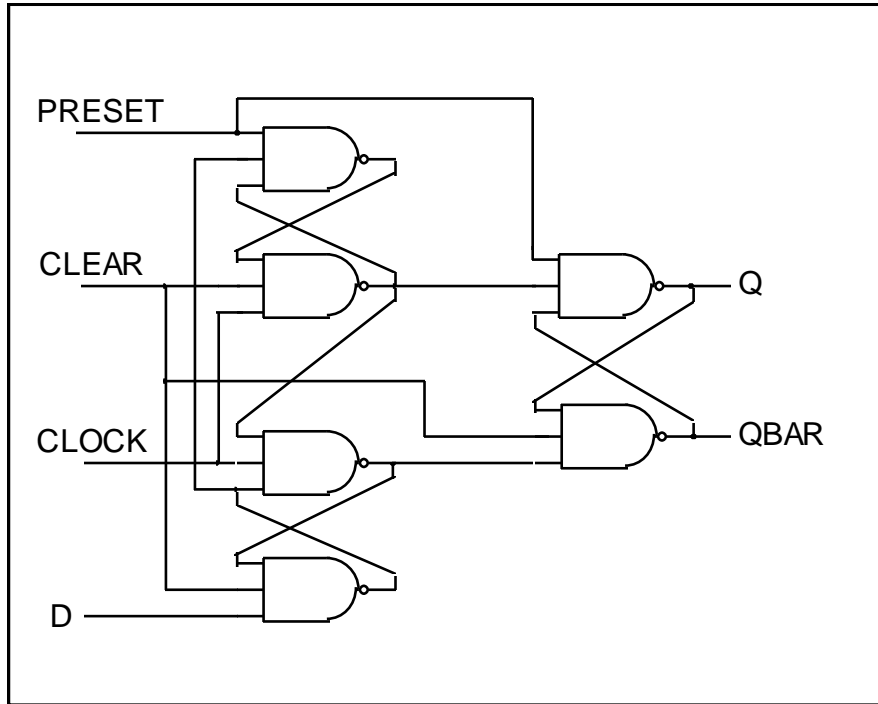
Figure 2: Schematic of internal logic of '74 Edge Triggered D flip-flop