Boundary Scan Register of the DSP56302 and DSP56303

The listings of the Boundary Scan Register (BSR) in the DSP56303 and DSP56302 User's Manuals are incorrect, (in both manuals, in Section 11.5, Table 11-2, pages 11-13 to 11-18). The BSR on both chips is identical, and the correct listing is:

Bit #	Pin Name	Pin Type	BSR Cell Type
0	$\overline{\text{IRQA}}$	Input	Data
1	$\overline{\text{IRQB}}$	Input	Data
2	$\overline{\text{IRQC}}$	Input	Data
3	$\overline{\text{IRQD}}$	Input	Data
4	D23	Input/Output	Data
5	D22	Input/Output	Data
6	D21	Input/Output	Data
7	D20	Input/Output	Data
8	D19	Input/Output	Data
9	D18	Input/Output	Data
10	D17	Input/Output	Data
11	D16	Input/Output	Data
12	D15	Input/Output	Data
13	D[23:13]	—	Control
14	D14	Input/Output	Data
15	D13	Input/Output	Data
16	D12	Input/Output	Data
17	D11	Input/Output	Data
18	D10	Input/Output	Data
19	D9	Input/Output	Data
20	D8	Input/Output	Data
21	D7	Input/Output	Data
22	D6	Input/Output	Data

Bit #	Pin Name	Pin Type	BSR Cell Type
23	D5	Input/Output	Data
24	D4	Input/Output	Data
25	D3	Input/Output	Data
26	D[12:0]	—	Control
27	D2	Input/Output	Data
28	D1	Input/Output	Data
29	D0	Input/Output	Data
30	A17	Tri-State	Data
31	A16	Tri-State	Data
32	A15	Tri-State	Data
33	A[17:9]	—	Control
34	A14	Tri-State	Data
35	A13	Tri-State	Data
36	A12	Tri-State	Data
37	A11	Tri-State	Data
38	A10	Tri-State	Data
39	A9	Tri-State	Data
40	A8	Tri-State	Data
41	A7	Tri-State	Data
42	A6	Tri-State	Data
43	A[8:0]	—	Control
44	A5	Tri-State	Data
45	A4	Tri-State	Data
46	A3	Tri-State	Data
47	A2	Tri-State	Data
48	A1	Tri-State	Data
49	A0	Tri-State	Data

Bit #	Pin Name	Pin Type	BSR Cell Type
50	$\overline{BG}$	Input	Data
51	AA0	Tri-State	Data
52	AA1	Tri-State	Data
53	$\overline{RD}$	Tri-State	Data
54	$\overline{WR}$	Tri-State	Data
55	AA0	—	Control
56	AA1	—	Control
57	$\overline{BB}$	—	Control
58	$\overline{BB}$	Input/Output	Data
59	$\overline{BR}$	Output	Data
60	$\overline{TA}$	Input	Data
61	$\overline{BCLK}$	Tri-State	Data
62	BCLK	Tri-State	Data
63	CLKOUT	Output	Data
64	$\overline{RD}$, $\overline{WR}$, BCLK, $\overline{BCLK}$, $\overline{BS}$	—	Control
65	$\overline{CAS}$	—	Control
66	AA2	—	Control
67	AA3	—	Control
68	EXTAL	Input	Data
69	$\overline{CAS}$	Tri-State	Data
70	AA2	Tri-State	Data
71	AA3	Tri-State	Data
72	$\overline{RES}$	Input	Data
73	HAD0	—	Control
74	HAD0	Input/Output	Data
75	HAD1	—	Control

Bit #	Pin Name	Pin Type	BSR Cell Type
76	HAD1	Input/Output	Data
77	HAD2	—	Control
78	HAD2	Input/Output	Data
79	HAD3	—	Control
80	HAD3	Input/Output	Data
81	HAD4	—	Control
82	HAD4	Input/Output	Data
83	HAD5	—	Control
84	HAD5	Input/Output	Data
85	HAD6	—	Control
86	HAD6	Input/Output	Data
87	HAD7	—	Control
88	HAD7	Input/Output	Data
89	HAS/A0	—	Control
90	HAS/A0	Input/Output	Data
91	HA8/A1	—	Control
92	HA8/A1	Input/Output	Data
93	HA9/A2	—	Control
94	HA9/A2	Input/Output	Data
95	HCS/A10	—	Control
96	HCS/A10	Input/Output	Data
97	TIO0	—	Control
98	TIO0	Input/Output	Data
99	TIO1	—	Control
100	TIO1	Input/Output	Data
101	TIO2	—	Control
102	TIO2	Input/Output	Data

Bit #	Pin Name	Pin Type	BSR Cell Type
103	HREQ/TRQ	—	Control
104	HREQ/TRQ	Input/Output	Data
105	HACK/RRQ	—	Control
106	HACK/RRQ	Input/Output	Data
107	HRW/RD	—	Control
108	HRW/RD	Input/Output	Data
109	HDS/WR	—	Control
110	HDS/WR	Input/Output	Data
111	SCK0	—	Control
112	SCK0	Input/Output	Data
113	SCK1	—	Control
114	SCK1	Input/Output	Data
115	SCLK	—	Control
116	SCLK	Input/Output	Data
117	TXD	—	Control
118	TXD	Input/Output	Data
119	RXD	—	Control
120	RXD	Input/Output	Data
121	SC00	—	Control
122	SC00	Input/Output	Data
123	SC10	—	Control
124	SC10	Input/Output	Data
125	STD0	—	Control
126	STD0	Input/Output	Data
127	SRD0	—	Control
128	SRD0	Input/Output	Data
129	PINIT	Input	Data

Bit #	Pin Name	Pin Type	BSR Cell Type
130	$\overline{DE}$	—	Control
131	$\overline{DE}$	Input/Output	Data
132	SC01	—	Control
133	SC01	Input/Output	Data
134	SC02	—	Control
135	SC02	Input/Output	Data
136	STD1	—	Control
137	STD1	Input/Output	Data
138	SRD1	—	Control
139	SRD1	Input/Output	Data
140	SC11	—	Control
141	SC11	Input/Output	Data
142	SC12	—	Control
143	SC12	Input/Output	Data