Rensselaer Polytechnic Institute
Computer Hardware Design – ECSE 4770

Lab Assignment 3 – Altera Richards Controller and Logic Analyzer Laboratory
Rev.F

Introduction

This laboratory assignment is an introduction to digital hardware design using a state machine. The system specifically uses a Richards Controller, a counter-based state machine implementation that is implemented in a Field Programmable Gate Array.

Objectives

- Design of digital hardware using block diagram/schematic entry
- Construction and debugging of digital hardware
- Use of a logic analyzer as a debugging tool
- Role and operation of state machines in digital design.
- Use of the Altera FPGA hardware and design tools.

Preparatory reading and other references

Charles L. Richards, , "Easy way to design complex program controllers". *Electronics* v.46 no.3, Feb 1, 1973, p107-113. (Controllers.pdf, located in the lab2 folder)

Quartus II Tutorial (located on the course web page).

"Logic Analyzer Operation", CHD course handout or located on the course web page folder.

Altera DE2 User Manual.

Procedure

Design requirements

The pre-lab assignment for this lab is to design a Richards Controller suitable for controlling an electronic stopwatch. The pre-lab **must** include, but is not limited to:

1. State Diagram
2. Logic Diagram
3. Description of internal controller operation
4. Timing Diagrams
5. Richards flowchart

Implementation

1. Use the TTL equivalent macros to implement your controller in a Altera FPGA. Demonstrate that the full functionality has been reproduced.

2. Optionally, reimplement the controller with the high-level constructs available in the design entry tools, such as an HDL or state machine capture.

Report Requirements

The final lab report must contain the following:
1. Revised logic diagram of the design built. Minor changes should be indicated in red on the original diagram, however if a major redesign was required a completely new diagram should be included
2. Description of the correct internal operation of the controller
3. A concise description of the debugging process
4. Description of the necessarily revisions to the original controller design
5. Timing diagrams for the final version
6. A copy of the pre-lab for the design use

General Description of the Stopwatch

The Richards Controller designed in this lab will control an electronic stopwatch. The stopwatch will be capable of storing up to 15 split times (instantaneous copies of the elapsed time) while maintaining the running time or a split time; and 15 address switches to determine which split is to be saved, viewed, or started.

The following portions of the controller are to be designed for this lab:
1. The stopwatch controller
2. The controller power-up reset circuitry
3. The debouncing circuitry for the START/STOP and COUNTER/SPLIT switches

The remaining stopwatch circuitry will be supplied in the lab as a pre-built module with a 16-pin DIP jumper providing connection.

Operating Scenario

The following example indicates the detailed operation of the RC stopwatch:

A runner wishes to find his/her lap times as he/she runs a track. A clock keeper has a Richards Controller stopwatch. The keeper turns on the watch; it automatically resets itself, displaying "00000". The runner starts while the timekeeper presses the START/STOP button and views the running time. At the end of the first lap, the keeper hits ADDRESS SWITCH #1 which causes the runner's first lap time to be saved in memory location 1. At the end of the second lap, the keeper hits ADDRESS SWITCH #2 and saves the runner's total time for the first and second laps ("the runners split timed") in memory location 2. The runner stops at the end of the fourth lap and the timekeeper hits the START/STOP switch to stop the clock.

The runner now wishes to see the time for the first lap, so the keeper presses the COUNTER/SPLIT switch, and then presses the address switch of the split the runner wishes to see: ADDRESS SWITCH #1. Then to show the runner the elapsed time after lap 2, the keeper presses ADDRESS SWITCH #2.

The runner wants to run on the track again, but he wants to start the stopwatch with the time he achieved for three laps. The keeper presses ADDRESS SWITCH #3, which was used to store the cumulative elapsed time at lap three, to get the split on the LED display. Now, when the runner starts the keeper will hit the START/STOP switch again and the clock will continue counting from the third lap split.

Stopwatch Function Summary

1. Power on: when power is applied, the controller should start in a known state and the counter display on the stopwatch module should read zero.
2. To start from zero:
    a. When the power is turned on and the START/STOP switch is pressed, the counter will start counting from zero.
    b. If the counters are stopped and the COUNTER/SPLIT switch has not been pressed to view any splits, the counter will be started from zero by pressing the START/STOP switch.
    c. If the counters are stopped and the COUNTER/SPLIT switch has been pressed to view splits, then the counter will start from zero when the COUNTER/SPLIT switch is pressed again followed by the depression of the START/STOP switch.
3. To stop the counter: the START/STOP switch is depressed while the counter is running.
4. To store a split time: press an ADDRESS SWITCH while the stopwatch is running. The split time will be stored in the memory location indicated by the ADDRESS SWITCH.
5. To recall a split time: (This can only be done while the counters are stopped.)
    a. Press the COUNTER/SPLIT switch and then the ADDRESS SWITCH corresponding to the desired split time.
    b. If the COUNTER/SPLIT switch was pressed to view a split previously, then only the ADDRESS SWITCH need be depressed to view any subsequent split time.
    c. If the COUNTER/SPLIT switch is pressed again the stopwatch should return to the "display counter" mode with the final stopped time displayed on the LED display.
6. To start from split: Follow the procedure previously defined to recall a split. When the desired start split is on the stopwatch LED display, the START/STOP switch should be pressed and the stopwatch should start from the displayed split.

Description of Stopwatch Hardware

A basic block diagram of the Richards Controller stopwatch is shown in Figure 1. As shown in figure 1, the stopwatch is made up of two sections. The first part is supplied in a "stopwatch module" in the lab. The second part must be designed and built by the student. The separation of these two parts is clearly delineated in the figure.
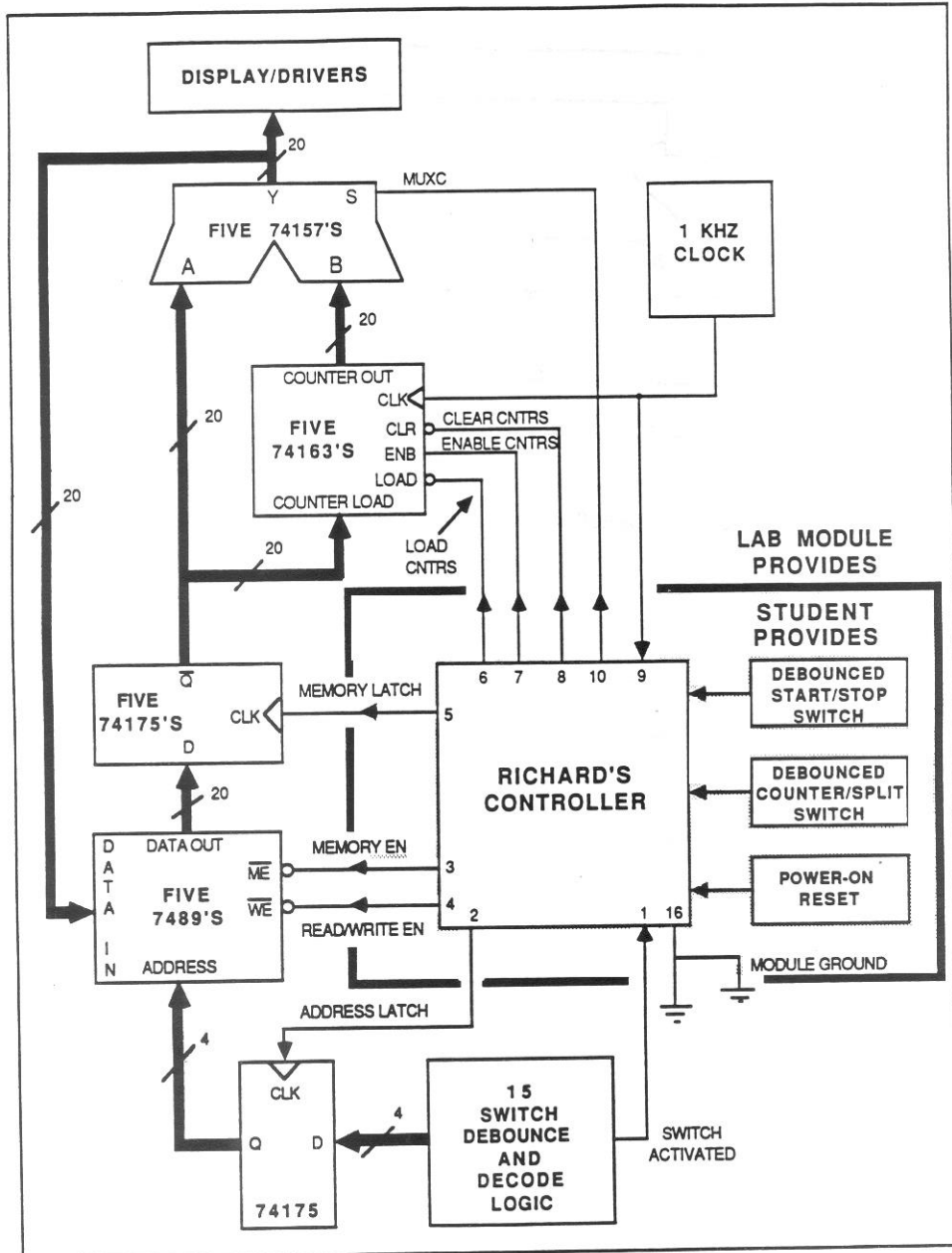

Figure 1: Stopwatch block diagram

Stopwatch module subsystems

The stopwatch module is composed of six major subsystems:
1. Display and drivers.
2. Multiplexer.
3. Counters.
4. Split memory.
5. Address switch logic.
6. 1 KHz clock.

The DISPLAY/DRIVERS block provides the necessary logic to decode BCD and drive a seven segment LED display.

The MULTIPLEXER block consists of five 74157 chips. This block selects the data that is applied to the LED display, which also leads to the memory input.

The COUNTERS block consists of five 74163 counter chips and some additional reset logic to provide the minutes, seconds/tenths/hundredths of a second format. All the counters work synchronously with the 1 KHz clock.

The SPLIT MEMORY block has two parts. The first, Main Memory, uses five 7489 memory chips while the second is memory latch consisting of five 74175 chips. The main memory holds the splits from the COUNTER block in the locations specified by the ADDRESS SWITCHES. The memory latch has two functions: it inverts the logic levels present in the main memory and it holds the last recalled split regardless of the output from the main memory.

The ADDRESS SWITCH logic provides the switch debouncing and encoding plus an address latch that holds the address generated by the ADDRESS SWITCHES. The timing of the ADDRESS SWITCH logic is shown in figure 2.

The 1 KHz clock is a 555 timer running at 2 KHz with a 7474 flip-flop acting as a divide-by-two stage. The 7474 divide-by-two circuit provides a symmetrical square wave clock of 1 KHz.

Stopwatch Module Interface

A ribbon cable with a 16-pin DIP connector is attached to the stopwatch module. This cable carries all of the interface signals needed to control the stopwatch module. The interface signals are listed in Table 1.

Table 1: Summary of Stopwatch Module interface signals

Pin #	Name	Mnemonic	Type	Loading
1	Switch Activated	SA	10 ms pos. pulse	N/a
2	Address Latch	ADDLATCH	Rising edge triggered	1
3	Memory Enable	ME	Active low	5
4	Read/Write	R/W	Write low	5
5	Memory Latch	MEMLATCH	Rising edge triggered	5
6	Counter Load	LD	Active low	5
7	Counter Enable	E	Active high	5
8	Counter Clear	CLR	Active low	5
9	1 kHz Clock	CLK	1 kHz square wave	N/a
10	Multiplexer Select	MUXC	Counter High	5
11-15	Unused	N/a	N/a	N/a
16	Ground	GND	N/a	N/a

SA provides a 10-ms positive pulse when one of the split memory address switches has been pressed. While SA is high, a valid address is presented to the address latch. The address switch timing is show in Figure 1.
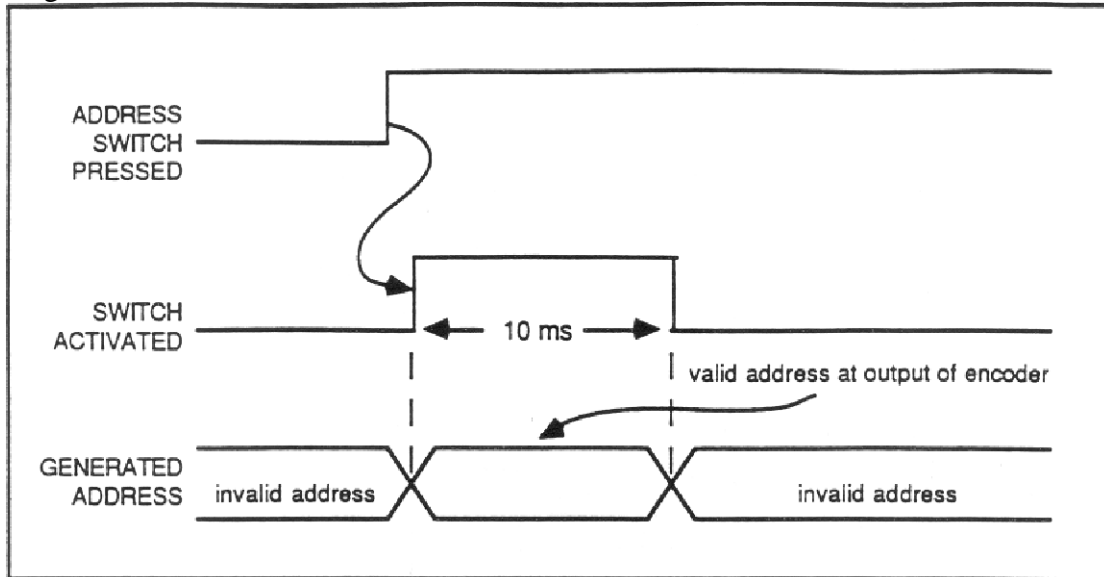

Figure 2: Address switch timing

ADDLATCH is a positive edge triggered signal that latches the data presented by the address switch matrix.

ME is an active low signal that enables the both the input and output ports of the split time memory.

RW is a signal which enables either the input or output port of the split time memory. When RW is high, the output is enabled and data can be read. When low, the input is enabled and data is written.

MEMLATCH is a rising edge triggered signal that latches the data read from the split-time memory.

LD is an active low signal the loads the counters with the output of the memory latch. The load is synchronous with the clock.

E enables the counters for incrementing with the clock. When low, the counters retain their last value.

CLR clears the counters, setting the output to zero. The clear is synchronous with the clock.

CLK is the 1 kHz clock for the entire circuit. The counters actually have a hidden 6th digit driven by this clock that has no display. This acts as a divide-by-10 circuit to drive the hundredths digit of the display.

When the MUXC signal is high, the multiplexers select the counter output; when low the memory output is selected.

GND is connected to ground on the stopwatch module. This is to ensure that the interface signals are in reference to a common ground.

Student Module

As shown in figure 1, the second part of the stopwatch is to be provided by the student as the prelab design assignment. This part includes the Richards Controller that will make the stopwatch function as described in the "Stopwatch Function Summary" section, the power-up reset logic, and the START/STOP switch and COUNTER/SPLIT switch debouncing. Switches are available for reset,

stop/start and counter split on the DE2 card. Interconnect between the DE2 card and the Richards box is provided on a protoboard. The interconnections and switch assignments are shown below.

Connection Table for Richards lab box to Altera DE2 card

Signal	Dip pin number(s)	DE2 (GPIO0) pin number	FPGA pin
SA	1	2	J22
ADDLATCH	2	4	E25
ME	3	6	F23
R/W	4	8	J20
MEMLATCH	5	10	F26
LD	6	16	G24
E	7	18	G25
CLR	8	20	H24
CLK	9	22	J24
MUXC	10	24	H26
GROUND	11-16	-	-

Switches and FPGA pin assignments

RESET (Sw17) Pin V2

COUNTER SPLIT (Key 0) Pin G26

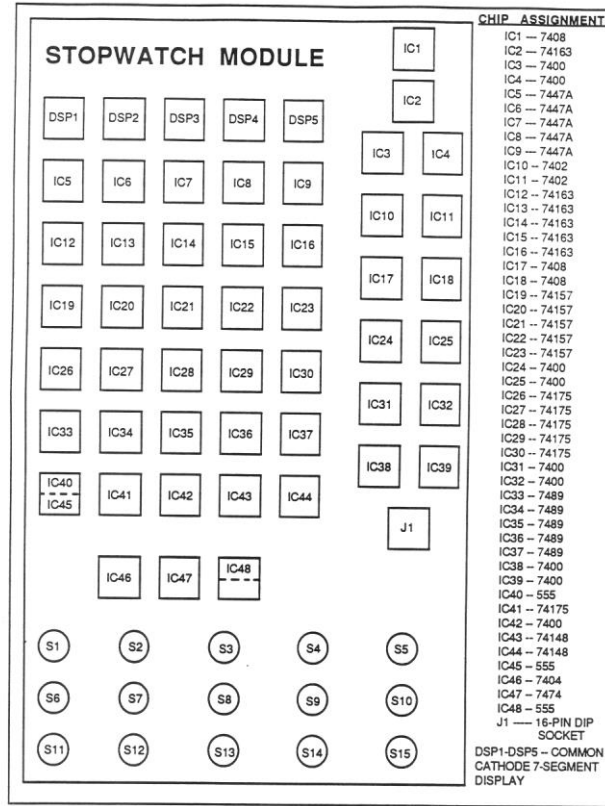Start Stop (Key 1) Pin N23

Stopwatch Module Detailed Diagrams

STOPWATCH MODULE

CHIP ASSIGNMENTS

IC1 — 7408
IC2 — 74163
IC3 — 7400
IC4 — 7400
IC5 — 7447A
IC6 — 7447A
IC7 — 7447A
IC8 — 7447A
IC9 — 7447A
IC10 — 7402
IC11 — 7402
IC12 — 74163
IC13 — 74163
IC14 — 74163
IC15 — 74163
IC16 — 74163
IC17 — 7408
IC18 — 7408
IC19 — 74157
IC20 — 74157
IC21 — 74157
IC22 — 74157
IC23 — 74157
IC24 — 7400
IC25 — 7400
IC26 — 74175
IC27 — 74175
IC28 — 74175
IC29 — 74175
IC30 — 74175
IC31 — 7400
IC32 — 7400
IC33 — 7489
IC34 — 7489
IC35 — 7489
IC36 — 7489
IC37 — 7489
IC38 — 7400
IC39 — 7400
IC40 — 555
IC41 — 74175
IC42 — 7400
IC43 — 74148
IC44 — 74148
IC45 — 555
IC46 — 7404
IC47 — 7474
IC48 — 555
J1 —— 16-PIN DIP SOCKET
DSP1-DSP5 — COMMON CATHODE 7-SEGMENT DISPLAY

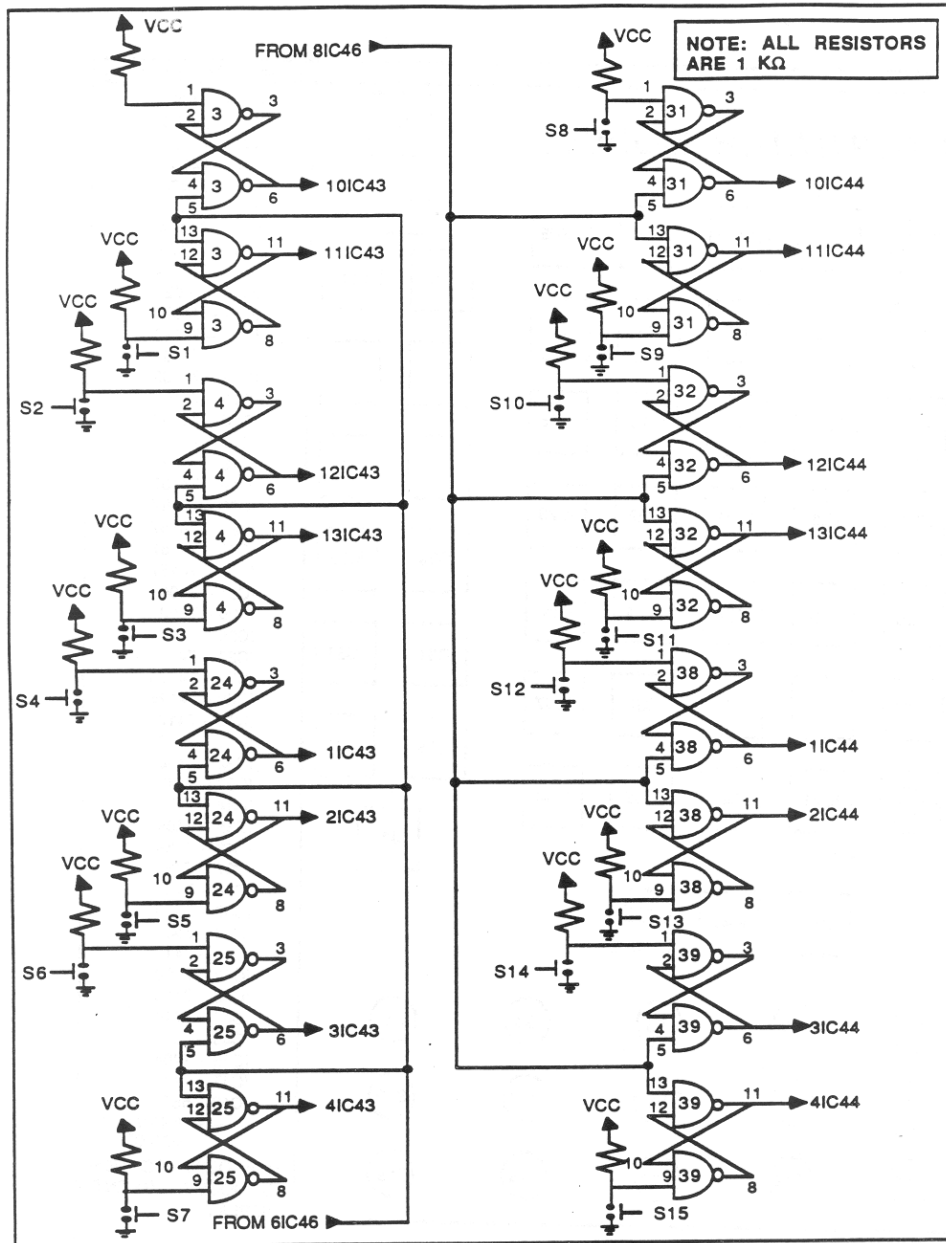**Figure 3: Board Chip layout**

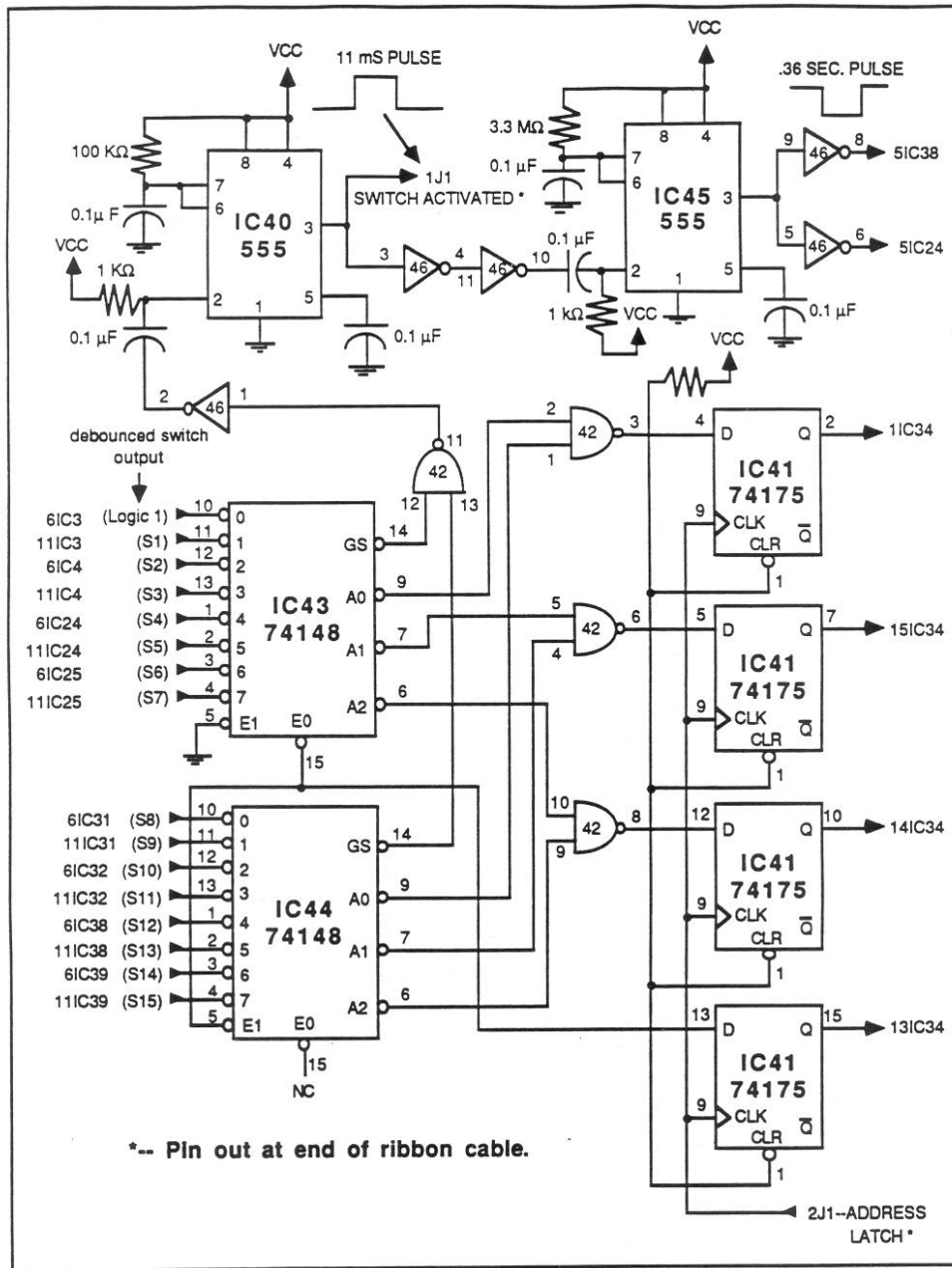**Figure 4: Address switch debouncing logic**

Figure 5: Encoding logic, SA signal generation, and address latch
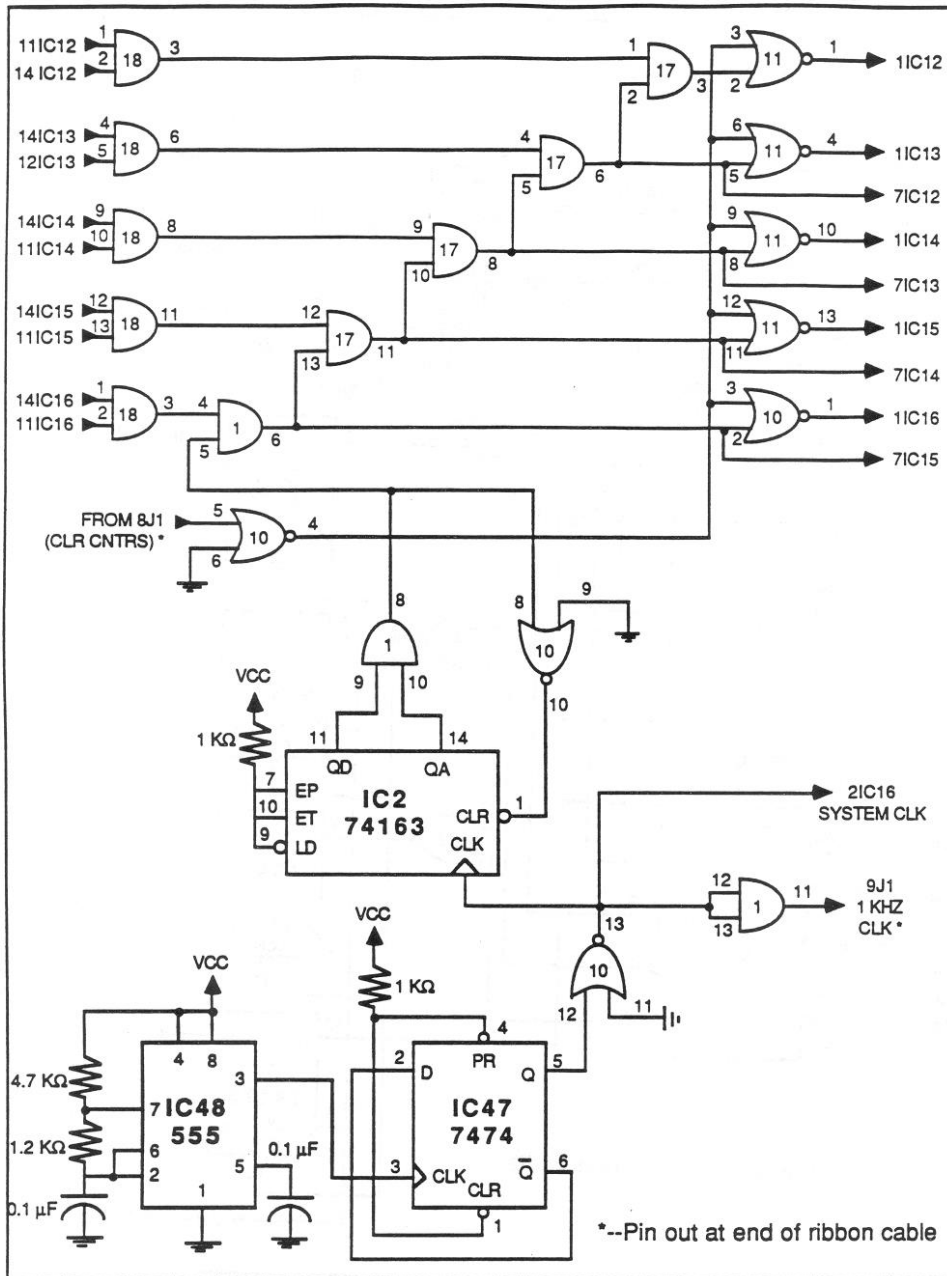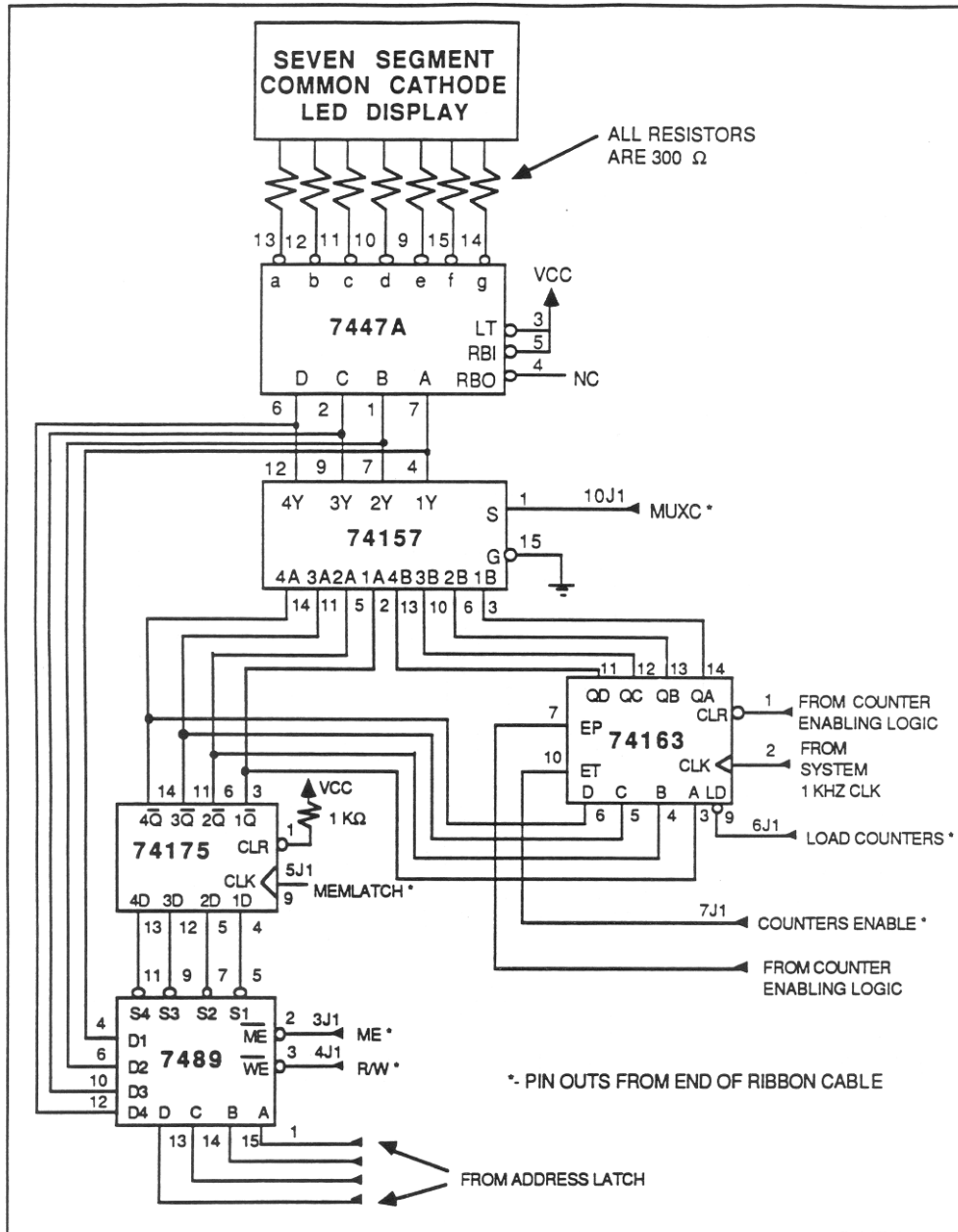
Figure 6: Counter enabling Logic and 1 kHz clock generator

Figure 7: One digit of stopwatch module