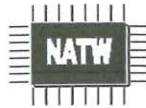
General Chair
Eugene Atwood – IBM
Vice General Chair
Kelly Ockunzzi – Marvell Semi
Program Chair
James Lloyd – SUNY Polytechnic Inst.
Vice Program Chair
Danella Zhao – Old Dominion Univ.
Tutorial co-Chairs
Carl Wisnesky – Cadence
Krishna Chakravadhanula - Cadence
Special Sessions Chair
Andy Laidler – ON Semiconductor
Panel Chair
Malinky Ghosh – IBM
Finance & Registration
Charles Thangaraj - Roger Willams U.
Ryan Patterson – Unisys
Xinghao Chen – IEEE
Ted Cooley - Cooley & Company
Local Arrangements
TBD
Publication Chair
Themistoklis Haniotakis – S. Illinois U.
Web Master & Publicity
Yu Zhang – Delphi Automotive
Fen Guan – GlobalFoundries
European Liaison
Patrick Girard – LIRMM, France

Program Committee
D. Armstrong - Advantest
R.I. Bahar – Brown Univ.
M. Brown – Mentor Graphics
Hari Chauhan – Analog Devices
Q. Lin - Broadcom
I. Harris – UC Irvine
M. Hsiao – Virginia Tech.
N. Karimi – Rutgers Univ.
S. Kundu – NSF/UMASS Amherst
J.C. Lo – U. Rhode Island
X. Lin – Mentor Graphics
Y. Ma - Advantest
M. Maniatakos – NYU
N. Nicolici – McMaster Univ.
S. Reddy – University of Iowa
J. Suzrez – Navy
J. Roehr – Test Consultant
V. Singh – IIT - Bombay
M. Slamani – GlobalFoundries
H.G. Stratigopoulos, CNRS/LIP6
M. Tehranipoor – U. of Florida
R. Singhal – Mentor Graphics
R. Tekumalla – Avago Tech
A. Veneris – U. of Toronto
X. Xiong – U. of Bridgeport
Y. Huang – Mentor Graphics
Z. Zilic – McGill Univ
Ujjwal Guin – Auburn U.
Uma Srinivasan – IBM Corp.

Steering Committee
Vishwani Agrawal – Auburn U.
Xinghao Chen – IEEE
Ted Cooley – Cooley & Company
Jennifer Dworak – SMU
Brion Keller – Marvell Semi
Martin Margala – UMASS Lowell
Karen Panetta – Tufts University
Paul Reuter – Mentor Graphics
Peilin Song – IBM Research
Tian Xia – Univ. of Vermont
Colin McDonough – IEEE Schenectady
Charles Rubenstein – IEEE R1



Call for Papers

29th North Atlantic Test Workshop
May 18-20, 2020
Albany, New York

Sponsored by the
IEEE Schenectady-NY Section & IEEE Region 1

http://natw.ieee.org

The IEEE North Atlantic Test Workshop provides a forum for discussions on latest issues relating to high quality, economical and efficient test methodologies and designs. The 29th NATW will feature a tutorial on Monday on the subject of VLSI reliability. In addition to traditional testing topics, the 29th NATW general theme is "Achieving Semiconductor Reliability." Major topics may include, but are not limited to:

- Analog, Mixed Signal & RF Testing
- Built-In Self-Test (BIST)
- Board and Package Level Testing
- Delay & Performance Testing
- Design Verification/Validation
- Diagnosis and Debug
- Fault Modeling/Simulation
- FPGA & Embedded Core Testing
- IDDQ Testing
- Machine Learning for Testing
- DFM, Defect Analysis & Defect-Based Testing
- Multi-Chip Module Testing
- Memory & MEMS Testing
- Nanotechnology Testing
- In-line and On-line Testing
- System-on-Chip (SOC) Test & Debug
- Test Quality/System Reliability
- Test Resource Partitioning
- Testing for Soft Errors/Defects
- Internet of Things (IoT)

The Program Committee invites authors to submit original, unpublished papers and panel proposals. Submissions may be in terms of extended summaries or full papers. Detailed instructions for submission can be found at the "*Author Information and Paper Submission*" link at http://natw.ieee.org. Papers found suitable for archival publication will be recommended by the program committee for submission to the "Journal of Electronic Testing: Theory and Applications (JETTA)," published by Springer. In addition, publication in IEEE Xplore is an option for authors who choose to do so.

Jake Karrfalt Best Student Paper Award

To encourage student participation in the testing research community, NATW has sessions dedicated to student presentations and includes a Best Student Paper Award.

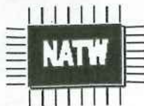
James Monzel Service Award: issued to individuals for dedicated service to NATW.

Important Dates: Submission – **02/21**/2020 / Notification of acceptance – **03/6**/2020
Submission of final papers – **04/26**/2020 / Submission of PPT presentations – **05/8**/2020

For general information, contact:
Eugene Atwood
IBM Mail Stop 93A
Bldg. 321, Flr. 1, Ofc. 1L10-20
2070 Route 52
Hopewell Junction, NY 12533
Phone: 845-592-6031
Email: eatwood@us.ibm.com

For program information, contact:
Prof. James Lloyd
SUNY Polytechnic Institute
NFE 4429
257 Fuller Rd.
Albany, NY 12203
Phone: 518-956-7062
Email: jlloyd@sunypoly.edu

Corporate/Academic Supporter packages available for 2020. Please see our website for more details. Corporate/Academic Supporters for 2019 included:



Workshop Theme 2020:

Achieving Semiconductor Reliability: Without Burn-In.

One of the holy grails of semiconductor manufacturing, revisited.

The practice of burning in semiconductor devices, in particular, assemblies of devices known as Systems On a Chip (SOC), is becoming increasingly difficult. Managing the amount of power dissipated by the SOC at elevated voltage and temperature is very challenging. Maintaining uniform temperature across the chip and ensuring that all logic participates in so called 'toggle coverage' to prevent over aging of chip regions or devices is difficult. EDA tools do not support toggle coverage evaluation or management of many different IP domains over the burn-in duration. For SOC burn-in, calling the burn-in oven an 'oven' is a mis-nomer, it should be burn-in refrigerator. Even with refrigeration, the amount of power is great enough to require duty cycle control of power. (lowering time average power) Reducing the duty cycle of the voltage acceleration increases burn-in duration, which increases cost. Sending SOC material into burn-in, some of which subsequently fails, forces incoming test and post burn-in test to be high quality. On the incoming side only material which will pass the out going test should be built. The built up module material will have a failure rate where detection of the failures requires a high quality test. Hence, burned-in material doubles the amount of time spent on a high quality tester and the cost of burn-in fail scrap can be significant.

Given that reliability statistics encompass the population of material, a method which eliminates or minimizes burn-in effort and improves the reliability statistics of the population is valuable, provided the method costs less than the cost of burn-in plus burn-in scrap. Several methods have been published {1-6] which address methods to minimize semiconductor dependence on burn-in. In addition to predictive methods, system designs are including real-time monitoring methods to identify failing memory or logic elements where the system responds by applying redundancy or partioning the failing logic outside of the functional operating space of the system. Redundancy and isolation have a cost in terms of requiring additional silicon or reduced performance, respectively.

The circumstances suggest that a best solution would be using in-line silicon with unique easy to test structures which predict the reliability of nearby material. Enhanced predictive methods which combine in-line based predictions with SOC test results and system redundancy suggest a robust cost effective path forward to reduce or eliminate traditional burn-in.

1. "D.W. Price and R.J. Rathert (KLA-Tencor Corp.). "Best Known Methods for Latent Reliability Defect Control in 90nm – 14nm Semiconductor Fabs". Nineteenth Annual Automotive Electronics Reliability Workshop. Novi, Michigan. April 2017".
2. A. Nahar, K. M. Butler, J. M. C. Jr., and C. Weinberger. "Quality Improvement and Cost Reduction Using Statistical Outlier Methods", *ICCAD*, 2009.
3. D. Drmanac, N. Sumikawa, L. Winemberg, L.-C. Wang, M. S. Abadir, ''Multidimensional parametric test set optimization of wafer probe data for predicting in field failures and setting tighter test limits,'' proceedings DATE, 2011, pp. 1-6.
4. Tadashi Sakamoto , Kazunori Yofu, and Takashi Kyuho, "New Method of Screening Out Outlier; Expanded Part Average Testing During Package Level Test", IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 30, NO. 4, NOVEMBER 2017
5. Robert Madge, Manu Rehani, Kevin Cota, W. Robert Daasch, "Statistical Post-Processing at Wafersort – An Alternative to Burn-in and a Manufacturable Solution to Test Limit Setting for Sub-micron Technologies.", Proceedings of the 20 th IEEE VLSI Test Symposium (VTS 02)
6. Walter Carl Riordan, Russell Miller, Eric R. St. Pierre, "Reliability Improvement and Burn In Optimization Through the Use of Die Level Predictive Modeling", IEEE 05CH37616 43rd Annual International Reliability Physics Symposium, San Jose, 2005

Parts Average Testing even has a Wikipedia entry.

https://en.wikipedia.org/wiki/Reliability_(semiconductor)#Methods_of_improvement

Parts Average Testing is a statistical method for recognizing and quarantining semiconductor die that have a higher probability of reliability failures. This technique identifies characteristics that are within specification but outside of a normal distribution for that population as at-risk outliers not suitable for high reliability applications. Tester-based Parts Average Testing varieties include Parametric Parts Average Testing (P-PAT) and Geographical Parts Average Testing (G-PAT), among others. Inline Parts Average Testing (I-PAT) uses data from production process control inspection and metrology to perform the outlier recognition function.[2][3]