Low $V_\pi L_\pi$ and Driving Voltage Interleaved Silicon Phase Shifter for Modulation Applications

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***Abstract*—Interleaved doped Mach-Zehnder Modulators (MZMs) are one solution to attaining higher modulation efficiencies compared with lateral junction structures, due to greater modal overlap with the depletion regions of the PN junctions. In this work, we present an interleaved Si modulator device design and process simulation based on a three-step ion implantation process that aims to obtain a realistic PN junction doping profile using a Monte Carlo simulation method. A high doping concentration on the order of 5×10^{18} cm^{-3} for the P and N regions is explored. Device simulations to track the carrier motion under different voltage biases are performed. Using equivalent medium theory, we calculated the modulation efficiency $V_\pi \cdot L_\pi$ of the interleaved Si modulator to be 0.19 V·cm under 1V reverse bias. This work is among the highest reported modulation efficiencies thus far in MZMs without photonic resonance structures.**

***Index Terms*—Silicon electro-optic modulator, interleaved, modulation efficiency, MZM.**

I. Introduction

ELECTRO-OPTICAL (EO) modulators are a key component for high-speed on-chip optical interconnects and optical fiber communication applications [1]–[5]. Various materials have been considered in pursuit of superb modulator performance including indium-tin-oxide [6], [7], lithium niobate [8], and 2D graphene [9]. Silicon based EO modulators have attracted considerable attention in the last two decades due to their low cost, small footprint, low energy consumption and strong compatibility with CMOS technology [5], [10].

Manuscript received April 18, 2022; accepted April 20, 2022. Date of publication April 29, 2022; date of current version May 4, 2022. This work was supported in part by the U.S. Army Research Lab under Grant W911NF-16-2-0049 and in part by AIM Photonics. *(Corresponding author: Z. Rena Huang.)*

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Digital Object Identifier 10.1109/JPHOT.2022.3170046

As silicon doesn't possess a linear electro-optic effect, Si EO modulators rely on the free carrier plasma effect to produce refractive index changes [11], [12]. The figure of merit, $V_\pi \cdot L_\pi$, measures the device modulation efficiency, where L_π is the phase shifter length and V_π is the bias voltage to generate a π-phase shift. Different PN-junction structures have been explored for efficient carrier modulation in Mach-Zehnder Modulators (MZMs). Conventional lateral MZMs consist of PN junctions with typical doping concentrations $<10^{18}$ cm^{-3} and carrier motions taking place perpendicular to the optical signal propagation direction [10]. This configuration limits the effective interaction of the optical field with the carrier plasma, resulting in limited modulator efficiency. A semiconductor-insulator-semiconductor capacitor-based (SISCAP) modulator reported good modulation efficiency with the price of high scattering loss due to partial optical waveguiding in a polysilicon layer [13]. In the past few years, interleaved PN junction structures [14]–[20] have been proposed and explored in which the PN junctions are placed with carrier motions parallel to the optical wave traveling direction, allowing the maximum light-matter interaction volume achieved without the use of any resonant structures as in [21]–[25].

Several works on interleaved modulators have reported enhanced modulation efficiencies [15]–[17]. In [14], a depletion type Si interleaved modulator was demonstrated with a $V_\pi \cdot L_\pi$ of 0.6 V·cm and a PN junction pitch size of 400 nm. A theoretical work on Si modulators has reported 0.24 V·cm with a doping level of 1×10^{18} cm^{-3} at a pitch size of 200 nm with an idealized PN junction profile assumption [15]. Increasing modulation efficiency or reducing $V_\pi \cdot L_\pi$ is the main goal of this work. A reduction in L_π implies a smaller device footprint that can save precious chip surface real estate and promote large array Si modulator integration. Smaller V_π values permit low-power driver circuit designs. Many low power CMOS circuits are designed to have a power supply of 1V, so Si phase shifters operating at $>$1V require on-chip transformers or power electronics circuitry to facilitate their usage [26]. Therefore, in this work, we also design the Si modulator to operate with a driving voltage of 1V.

By theory, a peak modulator efficiency can be achieved when the PN junction is fully depleted under bias, producing a maximum refractive index contrast under those two bias conditions. In this work, we will design and theoretically explore interleaved modulators that have high doping concentrations of $\sim5\times10^{18}$ cm^{-3} to achieve intense and spatially efficient

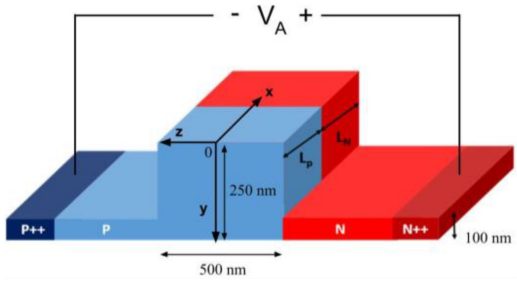

Fig. 1. Schematic of an unit cell of the interleaved PN junction structure.

plasma/light interaction. Ion implantation capabilities and process details are described to produce a realistic PN junction profile that matches the semiconductor manufacture process. Additionally, to improve junction performance, three ion implantation steps with peak doping concentrations targeted at different depths are explored in pursuit of a more uniformly doped junction.

II. Design of the Device

To design an optically efficient and minimal loss interleaved PN junction structure, specific design rules need to be considered and carefully controlled. EO modulators can be approximated using the Soref-Bennett model to estimate the changes in refractive index and absorption coefficients due to carrier concentration changes following empirical equations [11], [12]:

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8x10^{-22}\Delta N_e + 8.5x10^{-18}(\Delta N_h)^{0.8}] \quad (1)$$

$$\Delta\alpha = \Delta\alpha_e + \Delta\,\alpha_h = \left[8.5x10^{-18}\Delta N_e + 6.0x10^{-18}\Delta N_h\right] \quad (2)$$

where Δn_e and Δn_h represent the change in the real part of the refractive index caused by electron and hole concentrations, respectively, while $\Delta\alpha_e$ and $\Delta\alpha_h$ represent the absorption coefficients due to the electron and hole concentrations, respectively. In addition, ΔN_e and ΔN_h represent the carrier concentrations of electrons and holes, respectively. An initial refractive index value of $n = 3.45$ is used for undoped silicon.

A basic unit cell of an interleaved PN junction in a rib waveguide structure is presented in Fig. 1. with the width of the P region, L_p, and the width of the N region, L_n. The dimensions of L_p and L_n are determined by the ion implantation process and directly impact the modulation efficiency and the electrical properties of the device. Thus, it is critical to design the width dependent upon the desired doping concentration. Following (1) and (2) at $\lambda = 1550$ nm, a higher doping concentration leads to a greater change of refractive index, thus resulting in enhancement of the modulation efficiency.

The design of the unit cell should start from evaluating the depletion region dimensions based on the doping concentration and the driving voltage. Here we use an ideal abrupt PN junction for a numerical approximation of the depletion width, which provides a basis for the design of our device. The depletion width for an ideal abrupt PN junction can be approximated

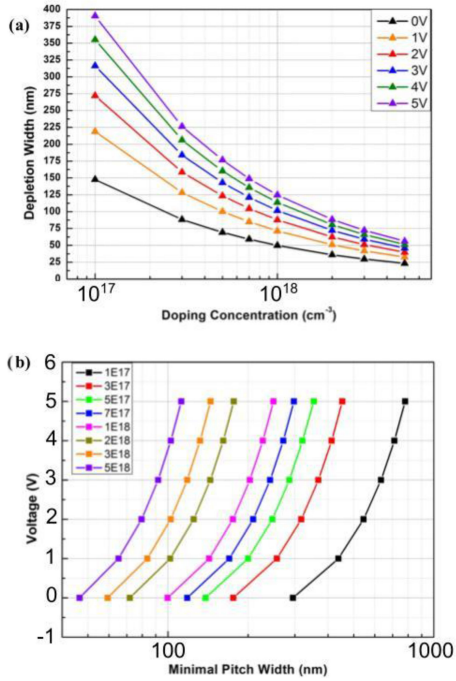

Fig. 2. Design rules to be followed for the interleaved PN junction structure: a) Depletion width based on the doping concentration and b) the minimum PN junction pitch width desired for various doping concentration of the unit cell.

by [27]:

$$W = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)[V_{bi}+V_A]} \quad (3)$$

where W is the depletion width, ϵ is the permittivity of the silicon (1.033×10^{-10} F/m), q is the elementary charge, N_A is the acceptor doping concentration, N_D is the donor doping concentration, V_A is the applied voltage, and V_{bi} is the built-in voltage, expressed as:

$$V_{bi} = \frac{kT}{q}\,ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (4)$$

where k is the Boltzmann constant, T is the temperature, and n_i is the intrinsic carrier concentration (9.65×10^9 cm^{-3} at room temperature [27]). For a quick performance estimation, full ionization rates are assumed for both the acceptors and donors in Eq. (3) and (4). Fig. 2(a)) shows depletion widths with respect to various doping concentrations and the driving voltages ranging from the equilibrium state up to 5V. Based on the choice of the depletion width and the bias voltage, the minimal pitch size of the PN junction, the sum of L_p and L_n, is presented in Fig. 2(b)) as the width needed to ensure full depletion of the carriers. This is twice the depletion width because each N/P region has depletion layers expanding from two ends due to the periodic nature of the device. At a relatively high doping concentration of $\sim 5\times10^{18}$ cm^{-3} where Si is degenerated doped, secondary effects such as band-gap narrowing, variable ionization rates, and ionized impurity scattering will need to be taken into consideration for realistic devices [27]. These effects are not considered in (3)

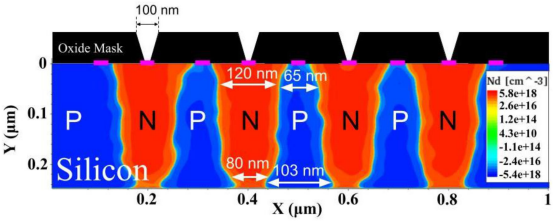

Fig. 3. The cross-sectional view of the interleaved PN junction with net effective dopant concentration (N_d). Here, the x-axis is along the optical signal propagation direction. The oxide mask is added manually to the carrier density map for illustration (not drawn to scale). The pink lines at Y = 0 represent the metal contacts in the simulation.

and (4) but will be included for the phase shifter modeling in Sentaurus.

For this work, the goal is to design the interleaved structure with a minimal PN junction pitch at a high doping concentration. The doping concentration was chosen at 5×10^{18} cm^{-3} and it corresponds to a minimal pitch size of 60 nm at 1V reverse bias as shown in Fig. 2(b)). A pitch size of 60 nm is closely approaching the limit of the fabrication capabilities, caused by the lateral straggle experienced during ion implantation [28]. In foundry-based silicon photonics fabrication, silicon doping is conducted through ion implantation, therefore most PN junctions formed are linearly graded junctions. The minimal pitch width calculations done earlier don't reflect realistic foundry fabrication process; but may provide a reasonable guidance for choosing doping levels for the beginning of more comprehensive simulations.

III. Device Modelling

A. Ion Implantation Model of the Waveguide

The ion implantation process is a key step to achieve a minimum interleaved pitch. It is modelled to determine the actual PN junction doping profile, and the outcome will vary depending upon the fabrication limitations of the resolution from the lithography technique and the physical implantation mask materials. The TCAD simulation was conducted through the Synopsys Sentaurus Process Package with the Monte Carlo ion diffusion model to predict the PN junction formation. Ion implantation modelling has five critical parameters that determine the junction formation: ion species, ion energy, tilt angle, annealing temperature, and ion implantation mask geometry. It has been shown that properly calibrated Sentaurus Monte Carlo simulations closely match experimental results for profiles of projected range and channeling [29].

For the ion species, boron and arsenic were selected for the p-type and n-type dopants respectively. A 310 nm layer of oxide was deposited on the top of the Si layer and patterned to form the implantation mask. This thickness of oxide is sufficient to block implanted ions with the ion energy levels chosen in this work [28]. A 100 nm opening is defined on the top of the oxide layer over the designated N and P regions, as shown in Fig. 3. Downward trenches of 82° are formed in the SiO_2 mask layer by the plasma etching process to create nano-windows with widths ~30 nm centered around x = 0.2 μm, 0.4 μm, 0.6 μm, and 0.8 μm. The entire wafer substrate was initially implanted with boron ions to produce P wells as well as background doping. A full furnace annealing was performed afterwards to ensure uniform P-type doping throughout the wafer along with recrystallization of the silicon lattice [28]. TCAD assisted process simulations were conducted in the same fabrication process order as in practice.

TABLE I
Ion Implantation Steps Used for Junction Formation

Step	Impurity	Ion Energy (keV)	Dose (cm^{-2})	Tilt Angle (deg)	R_p (nm)	$\Delta R_\perp$ (nm)
1	Boron	80	2.55×10^{14}	7	~270	~70
2	Arsenic	70	2.87×10^{13}	0	~43	~12
3	Arsenic	260	3.28×10^{13}	0	~160	~38
4	Arsenic	330	2.87×10^{14}	0	~200	~45

Following the p-type doping, the oxide masks were used with multiple arsenic ion implantation steps, each targeting peak concentrations at different progressive Si layer depths, allowing the formation of a more uniform vertical doping profile rather than a single Gaussian profile in the silicon layer. Arsenic was chosen specifically to reduce the ion thermal diffusion during the final annealing process once the impurities are set to form the nanoscale junction [30]. The doping parameters are outlined in Table I, each doping step used no rotation. Also mentioned in Table I are the projected range, R_P, and projected lateral straggle, $\Delta R_\perp$. The values are calculated with the Lindhard, Scharff, and Schiott (LSS) model and provided in [28] along with a more thorough explanation. The projected range describes the distance implanted ions travel parallel to the incident beam and the projected lateral straggle describes the statistical fluctuation along the direction perpendicular to the incident ion beam. The projected lateral straggle is of particular interest since it describes the lower limit of the interleaved pitch length. It is also important to note that the projected range is described without taking into consideration the projected straggle, the statistical fluctuation of the projected range parallel to the ion beam.

A commonly used tilt angle of 7° was used in step 1 to prevent channeling. This tilt angle presents a dense orientation of the crystal lattice with respect to the incident beam (approximately along the <763> direction) [28]. Subsequent steps do not need tilts as Arsenic atoms are heavy enough to prevent most channeling in Si [28].

Implanted ions are then annealed for 60 seconds at 1050°C with a rise time of 20 seconds and fall time of 60 seconds by using a rapid thermal annealing tool. Fig. 3 shows the resulting interleaved PN junction formation with the above process simulation conditions.

In the PN junction shown in Fig. 3, we observe that a junction pitch width of 180 nm is formed. Furthermore, it is noteworthy that the maximum peak concentration regions are 80 nm of N-well region and 65 nm of P-well region; and the effective PN junction width pitch is reduced to 145 nm due to graded doping profile. The peak concentrations in the N and P regions are $\sim5.8\times10^{18}$ cm^{-3} and $\sim5.4\times10^{18}$ cm^{-3}, respectively.

The active carrier concentrations in the wells are consistent throughout the silicon depth. For comparison, a single shot ion implantation following a similar step 3 recipe from Table I, with adjusted dosage to $\sim 3.3\times10^{14}$ cm^{-3} in order to closely resemble the doping concentration in Fig. 3 was evaluated. The single shot implantation model resulted in the n-type doping falling 30 nm short of reaching the bottom of the Si layer. Multi-step ion implantation process is frequently used in the CMOS industry to obtain desired doping profile at designed depth.

B. Electrical Model

Once the ion implantation model was created using the process simulations in Sentaurus, electrical simulations were performed using Sentaurus Device. The software package allows a Fermi-Dirac statistical approach for solving doped regions. Carrier recombination models used include Shockley-Read-Hall (SRH) recombination, Auger recombination, and surface recombination. A Philips unified model (PHUMOB) and velocity saturation models [31] were used to determine the mobility calculations and to represent the majority and minority carrier dynamics in the PN junction. Because of the carrier recombination and heavy doping used, the Slotboom Bandgap Narrowing (BGN) [31] and the doping dependent SRH recombination-generation model are also included in the simulations. In the simulation, the metal contacts shown in Fig. 3 are assumed to be ideal ohmic contacts.

The carrier transport model used is key in developing accurate PN junction simulations. In this work, we used the hydrodynamic model which includes carrier temperature gradients, compared to the drift-diffusion model which does not. The hydrodynamic model assumes carrier mobility as a function of the average carrier energy. Compared to the Monte-Carlo model, which represents carriers as computer particles, the hydro-dynamic model takes much less time and is less accurate, but sufficient for modelling of the device in this paper.

Simulations from Lumerical DEVICE were used to estimate the junction capacitance. The Lumerical 3D charge transport simulator uses the gummel method to solve a representative junction with uniform doping at levels of 5×10^{18} cm^{-3} and 6×10^{18} cm^{-3} for the P and N regions of the device, respectively. The width of the P and N regions used are 80 nm and 100 nm, respectively.

C. Optical Model

After the electrical model was simulated, the next step was to express the carrier density information into changes in refractive index and optical absorption. They are calculated by (1) and (2). After the carrier concentrations are mapped to refractive index values, we used the Finite Difference Eigenmode (FDE) solver in Lumerical to compute the effective index of the waveguide. The FDE solver solves Maxwell's equations on a cross-sectional mesh of the waveguide for various modes. A convergence test was done to verify that an appropriate simulation window size was chosen. We take the information calculated for the effective index for the fundamental TE mode along the segmented waveguide and apply effective medium theory to represent this as a continuous waveguide with a single effective index [32]–[35]. The equivalent effective index is computed every 10 nm along the propagation direction within one pitch of the device. This allows us to easily evaluate the modulation efficiency by comparing the equivalent effective index change when bias voltages are applied.

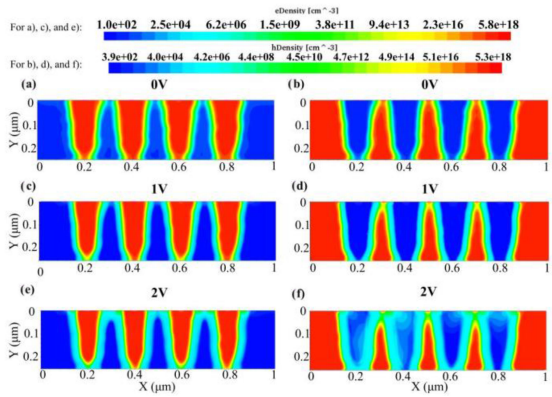

Fig. 4. (a), (c), (e) Electron density concentrations for different applied voltages and (b), (d), (f) Hole density concentrations for different applied voltages. Each cutline analysis is performed at z = 0.

IV. Results and Discussion

The electron and hole concentrations under various bias voltages are shown in Fig. 4. A strong depletion in the P regions was observed under a relatively small reverse bias of 1V. The depletion region increases from 27 nm to 40 nm when the reverse bias voltage is changed from 0V to 1V. This is achieved because of the high doping concentrations used for the device. Compared to a heavier doped device, lighter doping would require a larger reverse bias voltage to produce the same amount of carrier plasma change at the edge of the depletion layer for equal refractive index modulation. For example, referring to Fig. 2(a), a doping concentration of 5×10^{18} cm^{-3} undergoes a depletion region change of $\sim$10 nm when V_A changes from 0V to 1V. Compared to a lighter doping of 1×10^{17} cm^{-3}, the depletion region change in order to achieve the same amount of carrier plasma change is $\sim$500 nm, which requires a V_A change from 0V to 9V. Carrier concentration plots at 0V, 1V and 2V reverse bias conditions are provided in Fig. 4 for a more thorough demonstration of the device operation. Under high PN junction doping, Zener breakdown due to quantum tunneling effect in the junction will also occur at relatively lower reverse bias. To achieve a maximum index modulation, the modulator needs to avoid operation in the breakdown region. Here one period interleaved device is evaluated to provide an estimation of the modulation efficiency. Fig. 5 shows the calculated effective indices varying along the wave propagation direction. Equivalent medium theory allows us to represent this segmented waveguide as a continuous waveguide with a fixed, approximated index [32]–[35].

The phase shift per unit length can be approximated by integrating the differences in effective index over the propagation

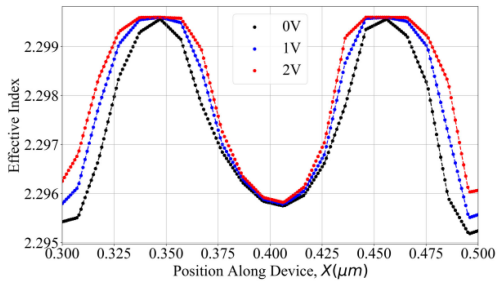

Fig. 5. The calculated effective index along the wave propagation direction within one period of the interleaved electrodes for different reverse biases.

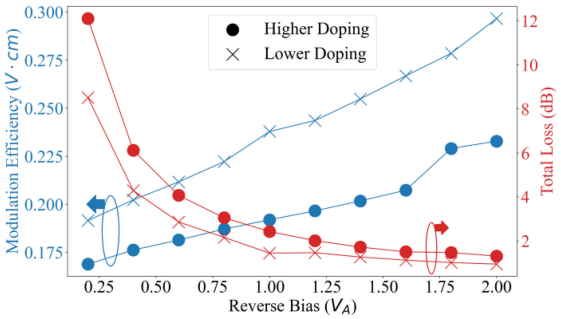

Fig. 6. The calculated modulation efficiency and total loss at different reverse bias voltages. Total loss shown refers to the free carrier absorption loss in L_π length. The traces labelled "Higher Doping" refer to the device created by the implantation steps in Table I and shown in Fig. 3. Traces labelled "Lower Doping" refer to a similar device with dosage levels adjusted, reducing the N-well doping level from ~5.8×10^{18} cm^{-3} to ~3.6×10^{18} cm^{-3}.

direction for one interleaved pitch [15]:

$$\Delta\varphi = \frac{2\pi}{2L\lambda}\int_0^{2L}\Delta n_{eff}(x)\,dx \tag{5}$$

where $\Delta\varphi$ is the phase shift per unit length, Δn_{eff} is the equivalent effective index change between 0V and the bias voltage operation, and 2L is the length of the pitch. More simply stated, weighted averages can be used to approximate the change in effective index. A more rigorous solution to the change in effective index is provided in [15]. For the proposed phase shifter, the Δn_{eff} between operation at 0V and 1V is calculated to be ~0.0004 following (1). The modulator phase shifter length L_π is calculated by $L_\pi = \frac{\lambda}{2\Delta n_{eff}}$. At $\lambda = 1.55$ μm, the estimated L_π is 1.9 mm, which gives $V_\pi \cdot L_\pi = 0.19$ V·cm. Fig. 6 shows modulation efficiency values for various bias voltages. Smaller biases provide more efficient modulation, but suffer from increased losses, also shown in the same figure. We compared the modulation efficiency with a slightly lighter doped device as shown in Fig. 6. The lower doped device exhibits a better $V_\pi \cdot L_\pi \cdot \alpha$ figure of merit, due to the absorption being included in the metrics. Here α is defined as the total absorption loss in L_π length due to plasma scattering. The lower doped phase shifter has a $V_\pi \cdot L_\pi \cdot \alpha$ value of 1.78 V·dB, while the higher doped phase shifter is 2.43 V·dB. Although the intention is for the device to be used as a phase shifter in a MZM, the large difference in loss between the unbiased condition and the reverse biased, shown in Fig. 6, suggests that the phase shifter can also be used as an electro-absorption modulator. Table II summarizes modulation efficiency from literatures on non-resonant interleaved Si modulators for comparison. To the best of our knowledge, it is the among the lowest reported $V_\pi \cdot L_\pi$ for a Si PN junction based non resonant optical modulator. Our simulated $V_\pi \cdot L_\pi$ is also compared to an ideal abrupt PN junction phase shifter calculated under 1V reverse bias using (1) – (3). The simplified PN junction model with $N_A = 5.4\times10^{18}$ cm^{-3} and $N_D = 5.8\times10^{18}$ cm^{-3} yields a $V_\pi \cdot L_\pi$ value of 0.10 V·cm, while a realistic doping profile modelled with Sentaurus yields a $V_\pi \cdot L_\pi$ value of 0.19 V·cm.

TABLE II
OVERVIEW OF SILICON INTERLEAVED MODULATORS

Reference	Pitch (nm)	Doping (cm^{-3})	$V_\pi \cdot L_\pi$ (V·cm)	Speed (GHz)
This Work	180	~5×10^{18} (peak)	0.19	6.8
Li et al. [15]	200	1×10^{18}	0.24	16
Goykhman et al. [18]	200	4×10^{17}	0.78	~17
Giesecke et al. [14]	400	N/A	0.6	5
Yu et al. [17]	500	2×10^{18}	0.62	<2.6

It is worth noting that a real interleaved phase shifter is a 3D structure while in the Sentaurus simulation, we only modelled the 2D device characteristics in x-y plane. A uniform carrier distribution is assumed in the z direction. Besides the interleaved PN junctions formed in the center waveguide along x-direction, unaccounted for junctions are also formed between the slab (100 nm in thickness) and the center waveguides along the z-direction, resulting in underestimation of the modulation efficiency. On the other hand, neglecting the small bias drop on the lateral P and N regions connecting the center waveguide with the P^{++}/N^{++} via contact regions would result in overestimation of the modulation efficiency. Increased modulation efficiencies have been demonstrated using photonic resonant structures [23]–[25], but these modulators suffer from limited optical bandwidths and complex operation schemes.

The propagation loss coefficient of the modulator was calculated by taking the carrier density information calculated by Sentaurus Device and applying equation (2). Once the material (n,k) data is imported into Lumerical, the FDE solver is used to provide an estimate on the propagation loss. A weighted average of the absorption coefficient along the propagation direction is calculated to estimate the total loss of the device. At higher reverse bias voltages, the depletion region increases, thus reducing free carrier densities in the waveguide, leading to smaller absorptive losses.

The capacitance at 1V reverse bias was calculated to be 4 fF/μm, leading to a total capacitance of 7.7 pF. This relatively high capacitance can be attributed to the high doping concentration and small pitch size used in the device [17]. The slab Si regions that connect the rib waveguide to the via and contacts constitute the major source of the resistivity in MZMs. A higher doping in the slab will give rise to lower resistance but higher absorption loss, as a portion of the optical field is carried in the Si slab region. Fixing the Si slab length at 1 μm [17], [18] and using an average doping $N_A = N_D = 5\times10^{18}$ cm^{-3}, we estimated the resistance to be ~3 Ω for the L_π length. The estimated RC time

limited bandwidth of the interleaved phase shifter is 6.8 GHz. The proposed interleaved phase shifter can be further optimized in doping and geometry to achieve the best speed, loss, and $V_\pi \cdot L_\pi$ performance.

V. Conclusion

In this work we report the detailed process steps and theoretically investigated an ion implantation based, small-pitch EO silicon modulator with relatively high doping concentrations of $\sim 5 \times 10^{18}$ cm^{-3}. Three ion implantation steps are used to obtain a more vertically uniform doping profile compared to a single ion implantation step. The carrier concentrations are mapped to refractive indices and absorption coefficients by using Soref's empirical equations [11], [12]. Lumerical MODE simulations using the FDE solver are then used to evaluate effective indices along the device. Applying equivalent medium theory, Δn_{eff} of the device between 0V and 1V reverse bias is estimated. The calculated L_π of the device is 1.9 mm, while a modulation efficiency, $V_\pi \cdot L_\pi = 0.19$ V·cm is obtained. The PN doping pitch size is 180 nm, amongst the smallest reported in literature. The tight interleaved P and N doping regions allow for strong depletion under a low driving voltage of 1V reverse bias, where the capacitance of the device was calculated to be 4 fF/μm, leading to a total capacitance of 7.7 pF with Lπ length. To conclude, in this work, using semiconductor processing simulation tools, we obtained a realistic doping profile of an interleaved PN junction cell that produces highly efficient modulation in Si.

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