Integration of inverted InGaAs MSM array on Si substrate through low temperature wafer bonding

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An array of inverted InGaAs metal–semiconductor–metal (MSM) photodetectors has been integrated into a silicon substrate using a low temperature In–Au wafer bonding technique. The total thickness of the bonding metal layers is less than 1 μm. It is shown that the photocurrent of the back illuminated InGaAs MSM photodetectors after bonding increases by 70% compared to the front illuminated MSM measured prior to bonding while the dark current reduces slightly after bonding.

Introduction: Integration of III–V optoelectronic devices on an Si CMOS compatible chip has been intensively explored for more than a decade [1]. The metal–semiconductor–metal (MSM) photodetector (PD), which can work very quickly while still maintaining a large area for alignment tolerance due to its low unit area capacitance, is believed to be a good candidate for chip optical interconnection applications [2, 3].

The mismatch in thermal expansion coefficients is considered one of the challenges in practice for integration of InGaAs MSM PDs on the silicon platform. It is thus desirable to conduct bonding at low temperature to reduce thermal stress at the interface. Huang *et al*. [2] presented a thin-film InGaAs MSM PD bonded to Si substrate through Au–Au bonding at a temperature of 200–300°C. However, this is a not a standard CMOS compatible process. In this Letter, we present the heterogeneous integration of an InGaAs MSM array (20 × 18) on a silicon substrate at a low bonding temperature of 200°C using a high yield, CMOS compatible process. After integration, the photocurrent of the inverted integrated PDs improves by an average of 70% compared with front illuminated MSM PDs tested prior to bonding. The dark current of the PDs after bonding has shown a small reduction. The total thickness of the bonding layers is less than 1 μm, which makes it an attractive approach for planar heterogeneous integration beyond MSM PDs.

MSM fabrication and integration: The MSM PDs were fabricated on an MBE grown InGaAs wafer, which has a layer structure of InAlAs /InAlGaAs /InGaAs /InAlGaAs/InAlAs/InGaAs (40 nm /50 nm /740 nm /50 nm /40 nm /200 nm) on a lattice matched InP substrate. The $In_{0.52}Al_{0.48}As$ has a bandgap of 1.47 eV, which serves as a cap layer to reduce the dark current of the MSM PDs. These MSM structures were patterned by standard photolithography, followed by an e-beam metal deposition of 30 nm Ti and 300 nm Au, which are referred to as layer 1 and layer 2, respectively, as shown in Fig. 1. The corresponding testing structure was fabricated on an Si wafer that consists of probe pads and wire connections for bonding and electrical testing. A 2 μm SiO_2 insulating layer was first deposited on the silicon wafer using plasma enhanced chemical vapour deposition (PECVD). It was followed by deposition of metal structures that consist of five layers: Ti/Au/Ti/In/Au (60 nm/50 nm/10 nm/400 nm/10 nm), referred to as layers 3–7, as shown in Fig. 1. The total thickness of the bonding layers including those on InGaAs MSMs and Si/SiO_2 is 860 nm.

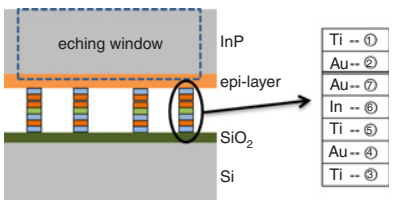

Fig. 1 *Inverted MSM integration process*

A Finetech® flip chip bonder was used to bond the InGaAs MSM to the Si/SiO_2 substrate through metal–metal bonding. The bonding took place under a pressure of 2 MPa for 45 min at 200°C. The next step was to remove the InP substrate of the MSM PDs using $HCl:H_3PO_4$ (1:1) to open a photodetection window. Citric acid was used to remove the InGaAs etching stop layer, leaving an InGaAs absorbing layer with 740 nm thickness.

Integration mechanism discussion: Low temperature bonding is the key to achieve low dark current of the MSM PDs because the Schottky contact degrades drastically at elevated temperature owing to migration of Ti and Au atoms into the semiconductor, resulting in intermixing of the metal atoms with the semiconductor crystal. Furthermore, the coefficient of thermal expansion (CTE) of an InGaAs wafer is significantly different from Si substrate, resulting in a large shear force at the interface if the bonding process occurs at high temperature. The In–Au liquid transient reaction at the bonding interface accounts for the physical mechanism of the low temperature bonding. It was shown that the reaction kinetics between gold (Au) and indium (In) is diffusion controlled, which follows the parabolic law [4]. The resulting inter-metallic compounds of In–Au reaction are determined by the weight percentage of indium of the bonding pads [5].

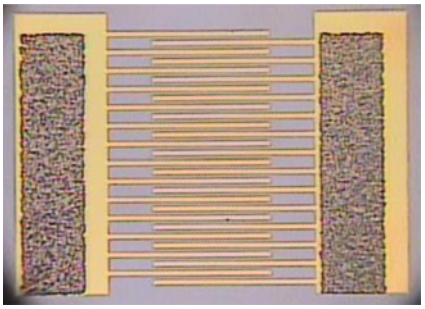

Fig. 2 *Image checked under microscope after separating bonded samples*

For the bonding pads on the silicon substrate, the top Au layer (layer 7) reacts with the indium (layer 6) during e-beam deposition, forming InAu grains on the sample surface, which prevents the oxidation of the indium layer. During the bonding process, these AuIn grains break further when the temperature rises above the melting point (156°C) of indium, making it possible for the Au layer (layer 2) on the InGaAs MSM to react with the In layer (layer 6) on the silicon wafer. The middle Ti layer (layer 5) between the Au layer (layer 4) and In (layer 6) on the Si/SiO_2 substrate works as a barrier layer to prevent the reaction between Au (layer 4) and In (layer 6) at room temperature [4]. During the bonding process when the pads are gradually heated from room temperature to 200°C, the Au in layer 4 can penetrate the Ti barrier layer (layer 5) and react with the indium (layer 6). As a result, the Au layers (layer 2 and layer 4) on both wafers quickly consume the indium of layer 6. As a result no indium spreading out is observed. Fig. 2 is a microscope image after we separated the bonded sample. The In–Au reaction leaves a dark region on the bonding pads. Additionally, it is worth mentioning that the bonding pads on the silicon wafer are intentionally designed slightly smaller than the pads in the MSM, as shown in Fig. 2. Thus, the bonding process can tolerate a small degree of indium spreading out if there is any.

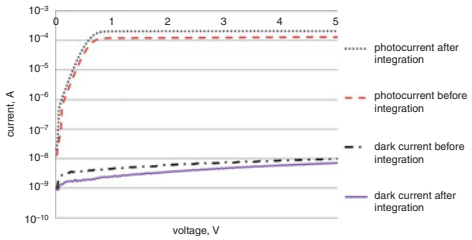

Fig. 3 *Dark currents and photocurrents measured before and after integration*

Test results and analysis: The photocurrents of the InGaAs MSM PDs were measured prior to and after bonding. Prior to bonding, the device was top illuminated through a lensed fibre at a wavelength of 1.55 μm. The power of the laser used in the test was 0.437 mW. After bonding, the growth substrate InP was removed and then the MSM PDs were tested with back illumination. The photocurrent of the back illuminated PDs after bonding was 70% higher than the front illuminated PD prior to bonding, as shown in Fig. 3. The ratio of responsivity between the front illuminated MSM PDs (R_1) and the inverted MSM PDs (R_2) can

be calculated by the following equation:

$$R_2/R_1 = (g + w)/g \quad (1)$$

where g is the finger gap and w is the finger width. As both g and w are chosen to be 3 μm in this work, the responsivity should improve 100% as predicted by (1). The discrepancy of 30% between theory and experiment is due to rough surface scattering of the inverted PDs after wet etching of the InP substrate.

To determine whether this bonding process affects the Schottky contact of the MSM, the dark currents of the MSM PDs were also measured before and after integration. As shown in Fig. 3, the dark current decreased slightly after integration. This might be attributed to the elimination of some defects at the interface during the heated bonding process.

Conclusions: Integration of inverted InGaAs MSM arrays on an Si substrate through low temperature wafer bonding has been demonstrated. The low temperature bonding is achieved owing to the In–Au liquid transient reaction at the interface. The photocurrent of the back illuminated MSM PDs has increased by 70% compared with front illuminated PDs prior to bonding. The dark current is reduced slightly after bonding, indicating that the Schottky contact of MSM remains unaffected. The reported InGaAs MSM fabrication and bonding process is compatible with standard CMOS processing, thus making it a suitable and manufacturable approach for heterogeneous integration of III–V MSM arrays on an Si CMOS chip.

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One or more of the Figures in this Letter are available in colour online.

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