The SOP for Miniaturized, Mixed-Signal Computing, Communication, and Consumer Systems of the Next Decade

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***Abstract*—From cell phones to biomedical systems, modern life is inexorably dependent on the complex convergence of technologies into stand-alone products designed to provide a complete solution in small, highly integrated systems with computing, communication, biomedical and consumer functions. The concept of system-on-package (SOP) originated in the mid-1990s at the NSF-funded Packaging Research Center at the Georgia Institute of Technology. This can be thought of as a conceptual paradigm in which the package, and not the bulky board, as the system and the package provides all the system functions in one single module, not as an assemblage of discrete components to be connected together, but as a continuous merging of various integrated thin film technologies in a small package. In the SOP concept, this is accomplished by codesign and fabrication of digital, optical, RF and sensor functions in both IC and the package, thus distinguishing between what function is accomplished best at IC level and at package level. In this paradigm, IC's are viewed as being best for transistor density while the package is viewed as being best for RF, optical and certain digital-function integration. The SOP concept is demonstrated for a conceptual broad-band system called an intelligent network communicator (INC). Its testbed acts as both a leading-edge research and teaching platform in which students, faculty, research scientists, and member companies evaluate the validity of SOP technology from design to fabrication to integration, test, cost and reliability. The testbed explores optical bit stream switching up to 100 GHz, digital signals up to 5–20 GHz, decoupling capacitor integration concepts to reduce simultaneous switching noise of power beyond 100 W/chip, design, modeling and fabrication of embedded components for RF, microwave, and millimeter wave applications up to 60 GHz. This article reviews a number of SOP technologies which have been developed and integrated into SOP test bed. These are 1) convergent SOP-based INC system design and architecture, 2) digital SOP and its fabrication for signal and power integrity, 3) optical SOP fabrication with embedded actives and passives, 4) RF SOP for high Q-embedded inductors, filters and other RF components, 5) mixed signal electrical test, 6) mixed signal reliability, and 7) demonstration of SOP by INC prototype system.**

***Index Terms*—Antennas, detectors, digital system-on-package (SOP), embedded components, embedded passives, embedded waveguides, electromagnetic interference (EMI), microvia, mixed signal design, optical SOP, power integrity, reliability, RF SOP, signal integrity, SIP, SOP, switches, test.**

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I. Introduction

In early 1970s, the single-chip packages on drilled-boards served the needs of the industry. The unparalleled performance needs of mainframes to meet the needs of corporate businesses demanded more integrated systems packaging technologies, giving rise to the birth of "MCM", initially with multilayer ceramic and subsequently with copper-polymer thin films in 1980 [1]. The MCMs, however, have not emerged to be widely accepted for two reasons: high cost, and lack of "Known Good Bare Die". To make it more cost effective, MCM thin-film technology began to be processed on larger boards, leading to build-up or surface laminar circuitry [2]. Even this technology, which is primarily used as thin-film multilayer wiring on packages such as BGAs, has not totally migrated to large-area boards. Independently, the so-called System-on-Chip or SOC became the dream of semiconductor companies in 1990s, depending less and less on packaging because of its high cost, bulkiness, and low performance and reliability. Over the next decade, it became clearer, however, that SOC for a complete system, presents fundamental, engineering, and investment barriers. This is about the time that portable electronics such as cell phones, laptops, PDAs, smart cards, and RF IDs began to emerge as primary consumer systems (see Fig. 1). The systems also began to be convergent, combining computing and communication functions in consumer-sized systems. This led the industry to invent a different MCM called SIP (system-in-package), one that could be stacked with multiple ICs or multiple package-stacked ICs and this time at much lower cost and size [3]. SIP can go one step further in embedding both active and passive components, but passive component embedding is largely of currently available bulky and multilevel thick film discrete components. This distinguishes SIP from SOP in that SOP involves embedding of both active and passives, but the passives are by incorporation of ultrathin films at microscale in the short term and nanoscale in the long term with a goal of increasing component density [4]–[7]. As pointed out in the first paper of this issue, all the above systems packaging technologies have one major shortcoming. They depend primarily on CMOS for the system characteristics and packaging to simply provide interconnections. The CMOS-based evolution and systems packaging evolution to SIP or MCM needed a different approach, one

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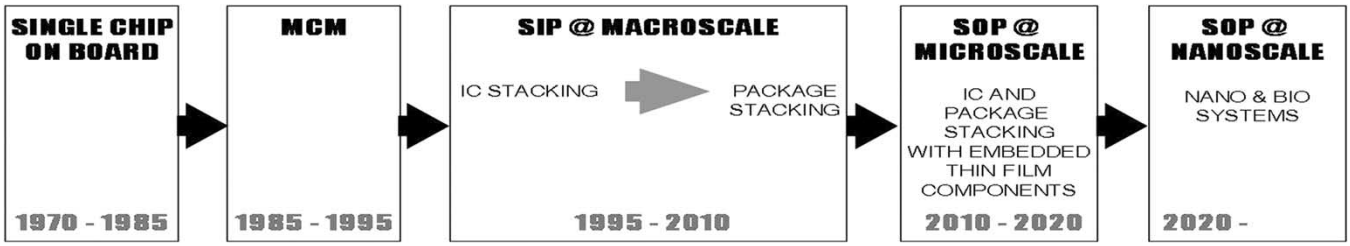


Fig. 1. Systems packaging has been evolving over decades consistent with systems needs as shown.

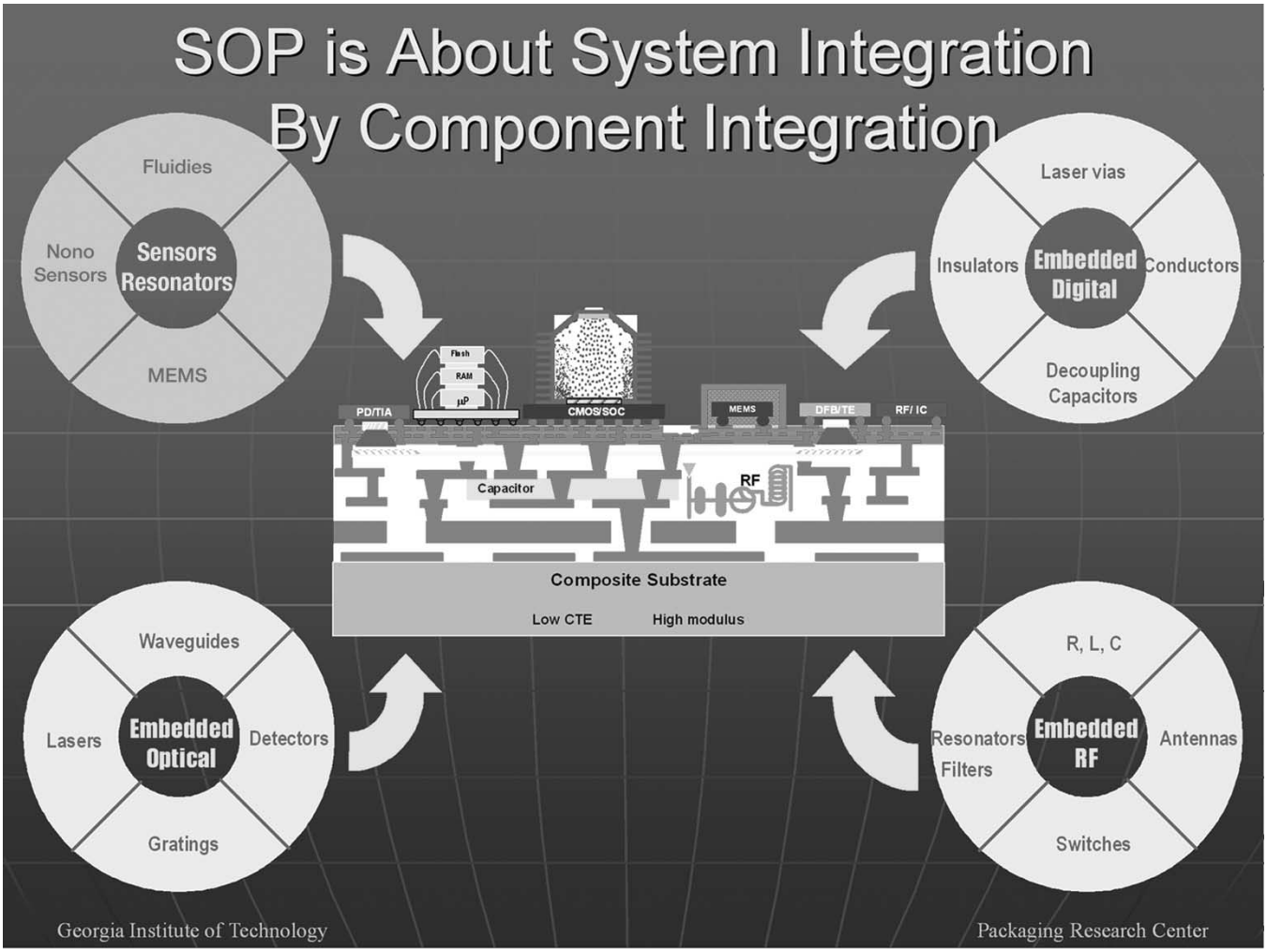


Fig. 2. SOP is about system integration by component integration.

that takes advantage of CMOS for what it is good for-namely transistors, and packaging for what it is good for—namely integration such as RF, Optical and certain digital functions. This is the conceptual paradigm that has become to be known as SOP or System-on-package, proposed by Prof Tummala in October 1993 [8] that led to the formation of the largest academic Center in the United States called the Pakaging Recearch Center (PRC) at Georgia Institute of Technology. In this concept, the package becomes the board and it is not simply for computing but also for communications and perhaps biomedical systems in highly miniaturized systems. This evolution depicting SOP for mixed signal systems based on embedding of components in thin-film form leading to highly miniaturized systems is shown in Fig. 2.

II. Mixed Signal SOP System Design and Architecture

The Georgia Tech's PRC has proposed what it calls an Intelligent Network Communicator (INC) system as a demonstrator of the SOP technology [9]. The INC system is driven by the emerging concepts that the future networks will have to deal with the optical, RF and digital signals in an unique and integrated system with new capabilities in both computing and communications. The INC system, therefore, is composed of three subblocks: the digital, analog, and optical sections, as shown in Fig. 3. Each of the subsystem blocks has been defined to deal with its own barrier issues. Since the entire system is built using a single SOP module platform, interfaces and isolation between

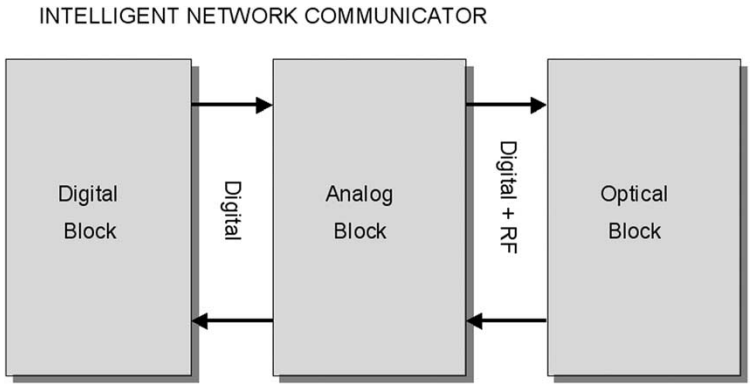


Fig. 3. INC system configuration in SOP technology.

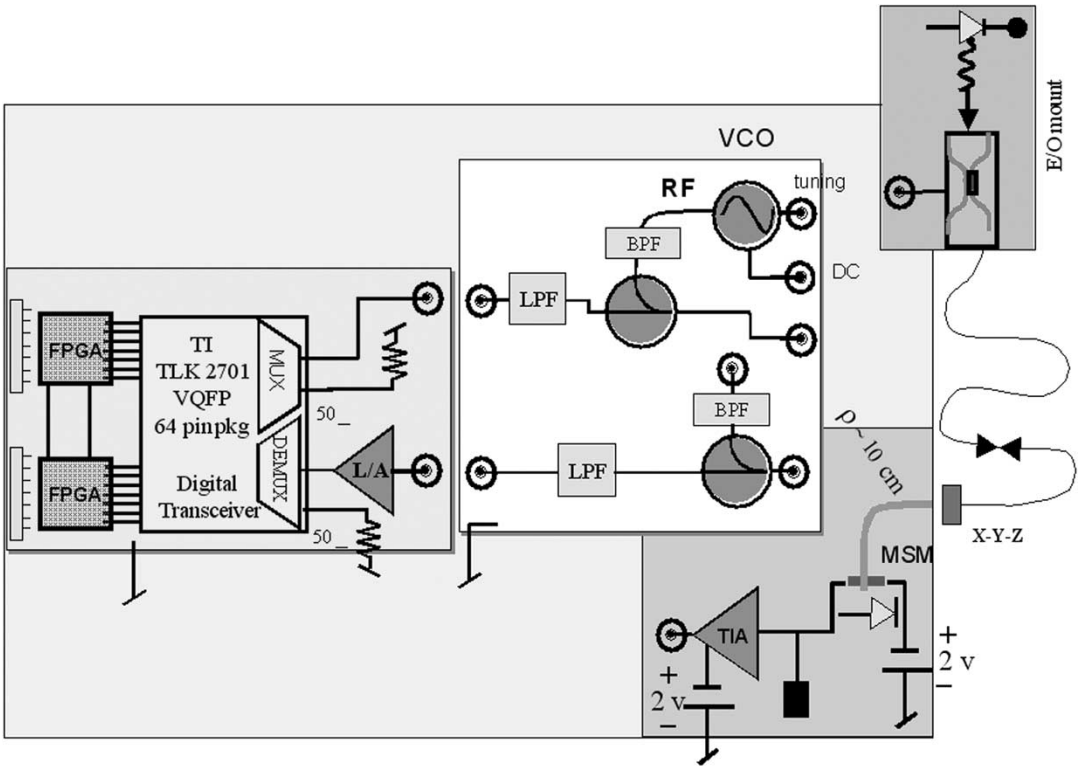


Fig. 4. INC mixed signal system with digital, optical, and RF blocks and interfaces.

the subsystem blocks become very important. The function of the INC is to transmit and receive high-speed digital and modulated RF signals, say wireless signal, concurrently over the optical channel. The system specification of each block has been defined to address the functional integration of that subsection. The target specification of each block in INC is summarized in Table I. The detailed configuration of the proposed system design is presented in Fig. 4. At the digital block, the multigigabit digital signal is generated by using the FPGA and compared with the received-signal after passing through the analog and optical blocks. The digital transceiver converts the multichannel input signals into a single data stream to feed to the analog block. The digital signal is then combined with modulated RF signal and transferred to optical block at the analog block. To accomplish this mission, a custom-designed mixed

TABLE I
TARGET GOAL

Digital Block	Data rate/channel	155 Mbps/Channel
	Aggregate date rate	2.5 Gbps (16 Channel)
Analog Block	Carrier frequency	5.8 GHz
	Signal Bandwidth	Single tone (VCO) / 20MHz (AWG)
Optical Block	O/E modulator	DC ~ 10 GHz (Mach-Zehnder)
	Photo Detector	DC ~ 10 GHz (Embedded)
	Light source	1530 ~ 1565 nm

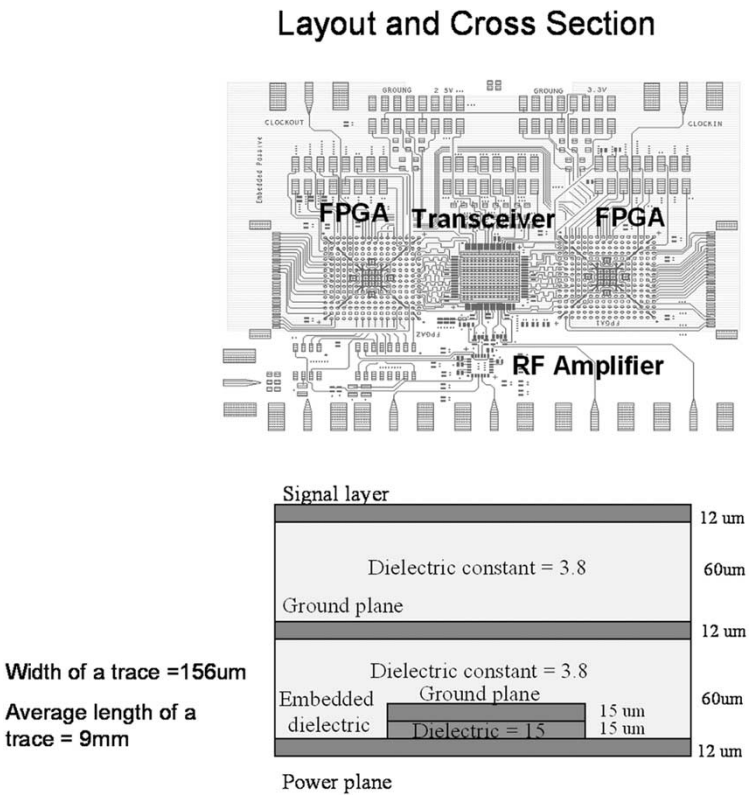


Fig. 5. Architecture of digital block. Layout and cross section of digital block.

signal combiner is used for the RF signal. The wireless LAN signal is generated by the electronic generation and a single carrier signal is generated by the voltage controlled oscillator. At the optical block, the mixed signal information is converted to light wave and transmitted through the embedded optical waveguide or optical fiber. The embedded photodetector converts the optical signal to electrical signal. At the receiver end of the analog block, the electrical signal obtained after passing the photo detector is separated into the digital and RF signals. The FPGA compares the generated-data and received-data to evaluate the system performance. To enable the single packaging solution, the various embedded components such as filters, mixed signal combiner and embedded optical waveguide have been implemented based on low-cost materials and process package technology on 300 mm boards.

III. Digital SOP: Design and Fabrication

The primary goal of any digital system is to ensure maximum throughput between IC's. One example that has plagued the industry for decades is the data path between microprocessors and memory or between multiple cores within a microprocessor. New architectures are being proposed for supporting terabit data rate speeds between processors (such as by Hofstee in this issue [10]. In addition, for memory channel, interconnection speeds greater than 3.2 Gb/s are being developed [11]. For the first time, the International Technology Roadmap on Semiconductors (ITRS) [12] is proposing the convergence of on-chip and off-chip clock speeds, with a goal of 5 GHz clock speed in the near future. These data rates are placing new challenges in the area of signal integrity, power integrity, and electromagnetic interference (EMI) in all systems including in SOP.

These challenges increase exponentially in mixed signal systems that integrate RF front ends with optical signaling and digital base-band processing. Though, the digital circuits operate at a slower speed compared to the predictions by ITRS in mixed signal systems, managing noise becomes a fundamental problem. Hence, along with supporting gigabit data rates on the interconnections, a noise free environment with isolation levels of less than -100 dB are required. This can be a difficult problem to solve, unless integrated technologies with good layout practices and clever architectures are used to minimize coupling. To reduce time to market, modeling tools supporting both prelayout analysis and post-layout verification become an integral part of the design flow. In this section, the design of the digital processing block in the mixed signal system shown previously in Fig. 2 is described in detail with emphasis on layout, modeling, technology integration, and measurements.

A. Design and Modeling

The physical layout and cross section of the digital block is shown in Fig. 5. The design uses microstrip lines on the top layer for signaling with ground and power plane layers beneath it. The 60 μm separation between the power and ground planes, provides for a low impedance path for the power distribution. An additional embedded decoupling layer using a nano-composite material (relative permittivity of 30) with a thickness of 10 μm

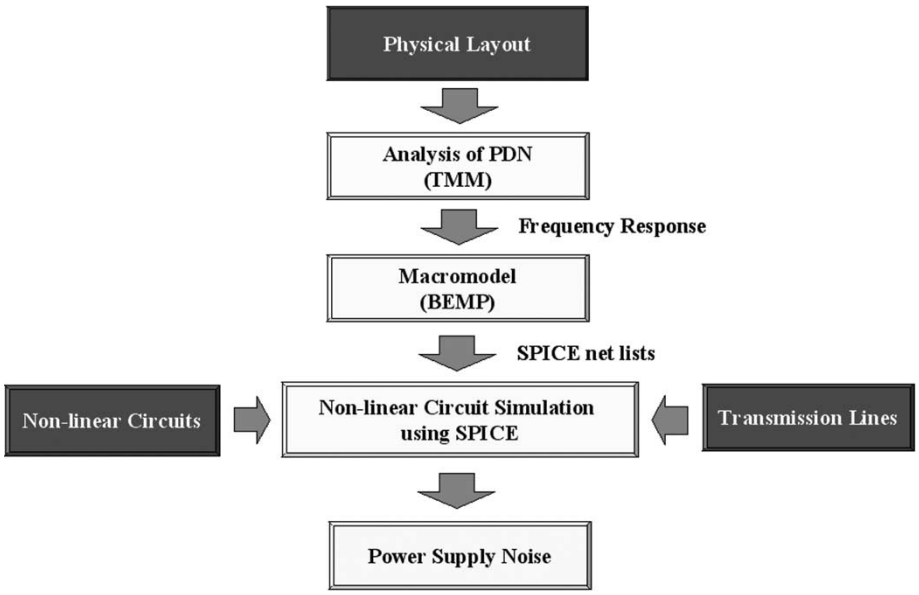


Fig. 6. Design and modeling flow.

enables further lowering of the impedance. This layer, which was patterned to minimize defects, acts as a low impedance path for the decoupling capacitors on the top layer and provides adequate isolation levels for a common power distribution network. The dielectric material used was epoxy $(\mathrm{er} = 3.8)$ with copper metallization. The design consists of split power islands to isolate the transmitter and receiver FPGA's from the transceiver chip. Ferrite bead, with an impedance of 600 Ω at 100 MHz was used to isolate the power planes and provide a common dc potential. A total of thirty-two 0402 decoupling capacitors with capacitance ranging from 1 nF to 47 μF were used in the design, to minimize the power supply noise. The microstrip lines with impedance of 50 Ω were terminated using resistors. A source synchronous design was used by transmitting the clock along with the data on adjacent interconnection.

Modeling tools developed at Georgia Tech were used to analyze the design for ensuring signal quality and noise minimization. The design and modeling flow is shown in Fig. 6, where the power distribution network (PDN) was first analyzed using the Transmission Matrix Method (TMM) [13] to extract the frequency response. The frequency response was then approximated using the Broad-band Efficient Macro-modeling Program (BEMP) [14] developed at Georgia Tech, to automatically generate a spice netlist of the power distribution. Nonlinear driver models and transmission lines were connected to the spice model of the power distribution to model the power supply noise. The layout in Fig. 5 was represented as a 14 port circuit for analysis, for extracting the coupling between various parts of the structure. At frequencies beyond 1 GHz, the inductance behavior of the power distribution is considerably reduced with embedded decoupling due to the thin separation between the plates of the capacitor. The time domain response of the power supply noise in the vicinity of FPGA 1 is a 10 $\times$ reduction in noise with embedded decoupling. The transceiver output is shown in Fig. 7, demonstrating the ability to support a 2.48-Gb/s differential serial channel.

IV. Digital SOP Fabrication

The digital SOP research focuses on ultrahigh-density wiring and low-loss dielectrics for high-speed signals and thin-film embedded decoupling capacitors for suppression of power noise.

A. High Speed Wiring and Dieletrics

The primary objective of SOP-digital wiring involves the integration of (a) ultralow-loss (~ 0.001) and thin film (5–10 μm) polymer dielectrics to achieve signal speeds of >10 Gb/s in the SOP package; and (b) multiple layers of ultrafine lines (5 μm) and stacked vias (10–15 μm) for wiring density >5000 cm/cm^2 and 50–100 μm area array pitch flip chip attach with Wafer Level Packages. The recently released 2003 ITRS roadmap [15] calls for >7.5 GHz package signal speeds and 100 μm flip chip pad pitch to satisfy 50 nm node requirements for future ICs. There have been significant developments in microvia and high-density build-up substrates and the state-of-the-art manufacturing processes use 25 μm line and space technology and 50–75 μm microvias [16]–[20]. Several low loss and low k polymers including epoxy, A-PPE, Avatrel, BCB, polyimide, and LCP have been evaluated at the PRC for signal speed and loss at frequencies up to 20 GHz. The typical properties of these materials are shown in Table II. The impact of dielectric loss on the signal speed is shown in Fig. 8 using measured eye diagrams at 5 Gb/s for low-loss polymers. For future SOP applications, thin film (10–15 μm) build-up dielectrics like BCB will enable the design of 50 Ω signals using 10 μm lines and spaces. The ideal dielectric for build-up SOP will combine the low loss of PTFE (~ 0.0001) for high speed with ultrathin-film processing for maximum interconnect density.

Area array I/O pitch of 50–100 μm requires escape routing with 5–10 μm lines and spaces and 10–15 μm stacked microvias. These dimensions have recently been demonstrated on low cost build-up PWB core substrates. Fig. 9 includes an extremely fine structure with 5 and 10 μm wide lines, 10 μm

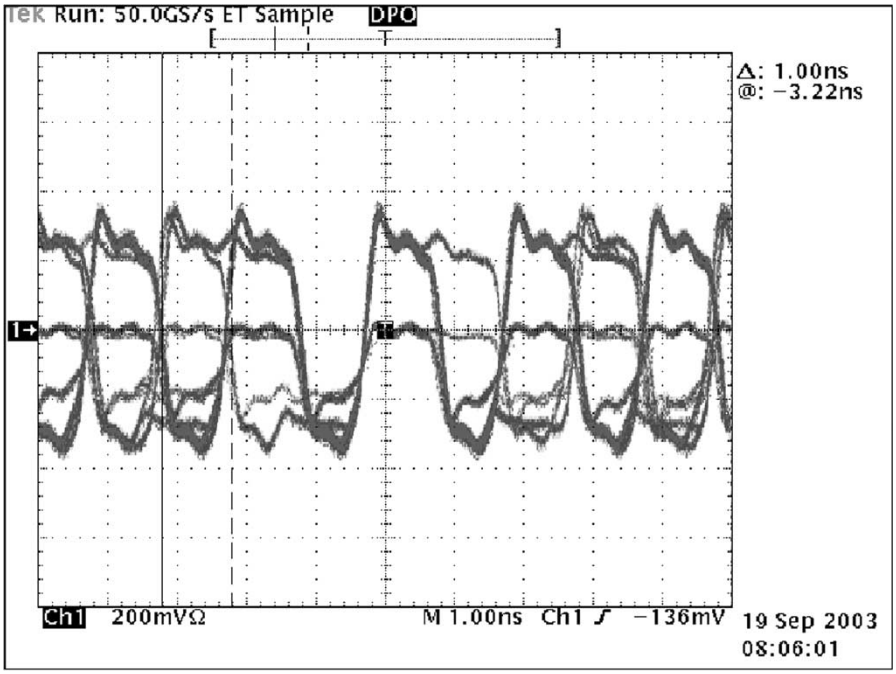


Fig. 7. 1. 6 Gb/s transceiver output.

TABLE II
PROPERTIES OF LOW-LOSS POLYMERS AT 1 GHz

Dielectric	Dielectric Constant	Tan δ
Epoxy	3. 8-4. 5	0.015-0.03
PPE	3. 2	0. 005
LCP	2. 8	<0. 003
Polyimide	3. 3-3. 5	0. 005
Avatrel	2. 5	<0. 001
BCB	2. 9	<0. 001

spaces, and $4\ \mu\mathrm{m}$ copper thickness. Precision photolithography with negative-acting liquid photoresists, glass photomasks and semi-additive plating processes were used to form these structures. A novel low-cost process for fabricating planar multilayer wiring with stacked microvias without any CMP process has been demonstrated. Fig. 9 includes a four metal layer of such a stacked via structure with fully filled copper studs of $50\ \mu\mathrm{m}$ diameter [21].

Packages for sub $-100\ \mu\mathrm{m}$ area array pitch, without large capture pads, require substrates with exceptional dimensional stability and high modulus to prevent warpage during multilayer thin film build-up. Fig. 10 summarizes the substrate warpage requirements needed to support ultrahigh wiring density and sufficient flatness for fine pitch assembly. Novel C-SiC large-area boards are being developed with CTE as low as 3–5 ppm/C and modulus as high as 450 GPa [22]. Such a material with exceptional dimensional stability will enable much tighter layer-to-layer registration and higher pad density. The CTE-match to Si is expected to help immensely to minimize stress on the solder joint and perhaps may eliminate expensive underfill processing.

B. Power Integrity by Embedded Decoupling Dielectrics

Embedded high-k dielectrics are particularly useful as mid-frequency decoupling capacitors for reducing ground bounce and simultaneous switching noise. Current surface mount discrete components are expected to reach their limit of operation in the few hundred MHz range due to the high lead inductance associated with solder interconnects. Novel polymer-ceramic nanocomposite dielectrics [23] have been used to fabricate thin film capacitors with a thickness of 10 $\mu\mathrm{m}$ and ε of 30 to achieve capacitance density up to 2.6 $\mathrm{nF/cm^2}$. Noise levels below 90 mV peak-to-peak have been demonstrated with this approach.

To achieve noise levels below 50 mV and to support power levels above 200 W, ultrathin-film high-k dielectrics are being developed using novel low temperature processes. Such synthesis methods as hydrothermal and sol-gel, with rapid thermal processing, have demonstrated films with thickness $<1\ \mu\mathrm{m}$ and capacitance densities of about 500 $\mathrm{nF/cm^2}$. The low process temperatures below 200 °C are well suited for integration on low cost organic SOP substrates. Fig. 11 shows a top view of a dense $\mathrm{BaTiO_3}$ film fabricated on metal foil using hydrothermal synthesis [24].

V. ORGANIC RF SOP

The SOP is a single component, multifunction package solution providing the needed system functions that include analog, digital, RF, optical and MEMS. The SOP also allows efficient integration of complete passive RF front-end functional building blocks, such as filters and power combiners. Recent development of thin-film RF materials and processes makes it possible to bring the concept of SOP into the RF world to meet

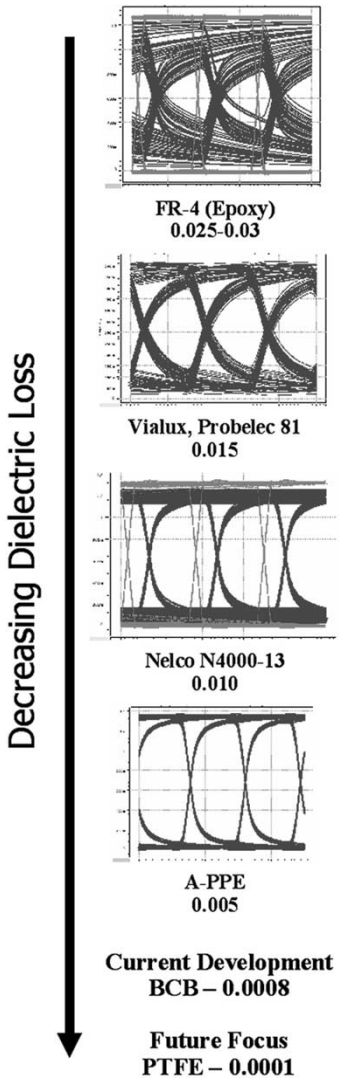


Fig. 8. Impact of dielectric loss on signal integrity for various thin-film materials (eye diagrams at 5 Gb/s).

the stringent needs in wireless communication area [25]–[28]. Critical issues such as wideband and low-loss interconnects, high-Q multilayer passives including R, L and C's [29]–[32], board-compatible embedded antennas and switches [33]–[35], low-loss and low-cost boards, efficient partitioning of MMICs, low crosstalk embedded transmission lines and single-moded packages, as well as design rules for vertically integrated transceivers are major barriers that have to be addressed over a wide frequency range. In addition, there exists a gap in the area of hybrid CAD needed to model novel functions that require fast and accurate modeling of electromagnetic, circuit, solid-state, thermal and mechanical effects.

Multilayer ceramic (LTCC) and multilayer organic (MLO) structures with liquid crystal polymer (LCP) technology [32] are used to embed passives efficiently, including high-Q inductors, capacitors, matching networks, low-pass and band-pass filters, baluns, combiners, and antennas. The 3-D design approach using multilayer topologies leads to high quality and compact components to support multiband, wider-bandwidth and multistandards in a very compact from factor and with low cost. A general system configuration of wireless transceiver is shown in Fig. 12. The breadth of integration is represented schematically in Fig. 13. The Transceiver module is composed of MMIC chipset: power amplifier (PA), low-noise amplifier (LNA), up and down mixer (MIX) and voltage controlled oscillator (VCO), and passive components: filter, antenna, and external high-Q discrete passive elements for stringent block such as PA and VCO. Some examples of passives built on SOP platform are represented in Fig. 14.

A. Multilayer Inductors

High-Qs at the frequency range of interest can be obtained by designing CPW inductors using multilayer organic technology. The CPW spiral inductor, depicted in Fig. 14, avoids via losses, has reduced dielectric losses and increased SRF. Also, the thick copper metallization in the packaging process make it possible to get a very high-Q. This decreases the shunt parasitic capacitance and reduces the eddy current flowing in the ground plane producing negative mutual inductance effect. As a result, higher Q and L_{eff} can be achieved. The CPW inductor demonstrates a Q of 182, SRF 20 GHz, Leff 1. 97 nH.

B. Embedded Filters

Several embedded filters were designed for the SOP process using epoxy materials for the build-up layers. The bandpass filter design for C band applications consists of a square patch resonator with inset feed lines, as shown in Fig. 14. The inset gaps act as small capacitors and cause the filter to have a pseudoelliptic response with transmission zeros on either side of the passband. This structure also has a tunable bandwidth. The length of the feed lines is determined by the input and output matching requirements. The length of the insets and the distance between them are the main controlling factors, effectively setting the size of the mode-splitting perturbation in the field of the resonator. Measurement result shows that bandwidth of 1.5 GHz and a minimum insertion loss of 3 dB at the center frequency of 5.8 GHz.

C. Combiners

To overcome the weak coupling at base band and the bandwidth limitation of conventional combiner, we modified the conventional coupled line coupler as vertical coupling structure in the SOP platform as shown in Fig. 15(a). The output port of the coupled line coupler is used as the input port for the RF signal and the isolation port is shorted to the ground. Also we designed ninth-order Bessel LPF at the input port for the base band, which performs as band stop filter for the 14 GHz RF signal and reflects the RF signal at the output of the LPF. We optimized the 14 GHz RF signal in-phase to obtain a constructive effect at the output port of the combiner by adjusting the embedded microstrip line which interconnects the LPF with vertical coupling structure. The design was finalized with the 3-D electromagnetic simulation software. The insertion loss of the RF signal at the output port of the combiner was measured as 1.9 dB. The isolation between port 1 and port 2 of the combiner was greater than 10 dB in base band and 38 dB at 14 GHz (VNA HP8510). These results satisfy the requirement for the proposed HDROS. 3 dB bandwidth of 7 GHz is achieved between port 1

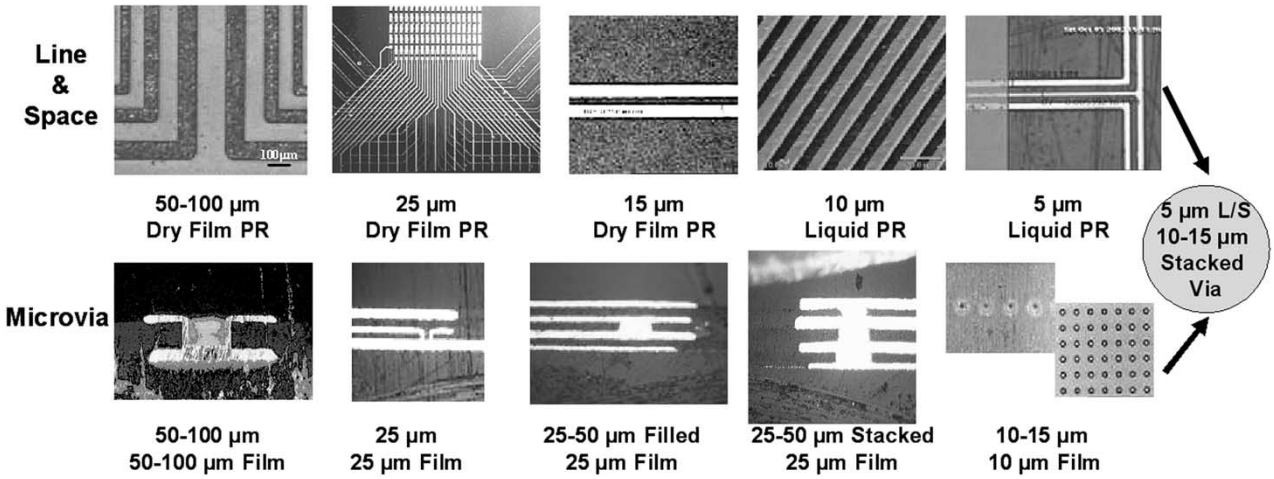


Fig. 9. Progress in lines and spaces, and microvias on low-cost organic SOP substrates at PRC.

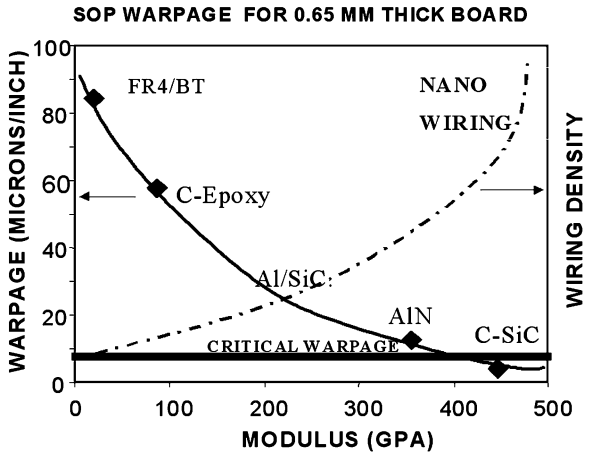


Fig. 10. SOP substrate warpage requirements for 0. 65 mm thickness.

and port 3. Fig. 15(b) shows the measured frequency spectrum at the output of the combiner when 7 Gb/s pseudorandom binary sequence (PRBS) with 14 GHz sinusoidal wave are sent. Fig. 15(b) also shows the measured eye opening of the 7 Gb/s PRBS at the output port.

D. Antennas

SOP can give flexibility to the transceiver module by integrating all functional blocks using the multilayer processes and the novel interconnection methods. One of the major issues, however, is how to integrate antennas with a high module efficiency and low cost, especially for the lowest frequencies of cellular communication and WiFi, that the physical antenna size is large. Fabricating an antenna directly on the package has the advantages of reduced feeder loss and size of the entire module. For the frequency band of the personal communication, WLAN and short-range broadband communications from 900 MHz to 6 GHz and 35–65 GHz, it is difficult to put an antenna into the module, since the size of the antenna becomes large. Moreover there are issues to be solved such as narrow bandwidth in ceramic packaging and interference between the antenna and other RF blocks in highly integrated module. The prototype antennas are designed to be integrated with the transceiver module and fabricated using multilayer package processes, such as MLO and LCPs [36]. The principle of novel soft–hard surfaces (SHS) was devised for the miniaturization and elimination of the substrate-crosstalk modes improving the efficiency of higher patch antennas [34] close to the free-space ones and suppressing the backside radiation by 10–15 dBs from 900 MHz and 1.55 GHz (GPS) to the short-range broadband (40–65 GHz). In addition, stacked-patch configurations allowed for the realization of broadband radiation performances.

E. Capacitors

Embedded high-k polymer/ceramic nanocomposite capacitors (dielectric constant 15–20) have been used primarily for the decoupling applications as discussed earlier. Currently, a capacitance density $\sim 1\ \mu\mathrm{F/cm}^2$ has been reported with a thin film of $\mathrm{BaTiO_3}$ using hydrothermal synthesis [37] that can be integrated with the SOP. Dielectric constant >1000 has been reported using metallic nanoparticles [38].

VI. Optoelectronics SOP

The focus of Optoelectronics SOP is the heterogeneous integration of optically active devices such as lasers, detector arrays, and laser amplifiers, and optically passives such as waveguides, gratings and beam splitters onto electrically interconnected mixed signal SOP, as shown in Figs. 16 and 17.

A. Integration of Embedded Active Optical Elements

The metal–semiconductor–metal photodetector (MSM-PD) has attracted attention from industry in recent years because of its simplicity in fabrication, lower capacitance than p-i-n photodiodes per unit area, and high alignment tolerance for assembly. In this research, the MSM-PD is independently grown, fabricated, and bonded directly onto organic boards and silicon chips. MSM-PDs are fabricated on an $\mathrm{In_{0.53}Ga_{0.47}As}$ layer which is grown on lattice-matched InP. The absorbing layer thickness can be varied between 100 and 740 nm to achieve the optimized responsivity and bandwidth [39], [40]. The Schottky electrode comb structure is patterned by standard photolithography and metallized with Ti/Pt/Au using e-beam evaporator. The InP growth substrate is removed by chemical etching, leaving a thin

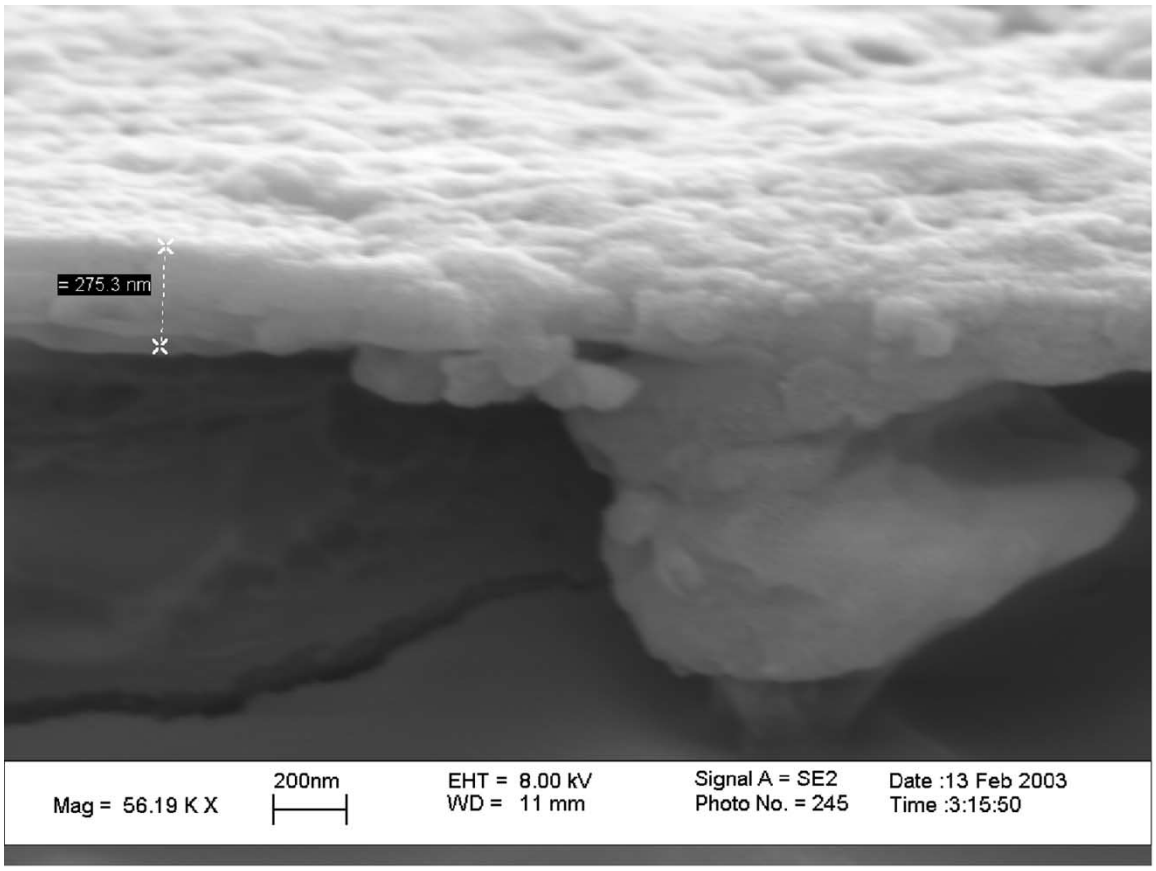


Fig. 11. SEM cross section of high $K(>350)$ hydrothermally grown film of $BaTiO_3$.

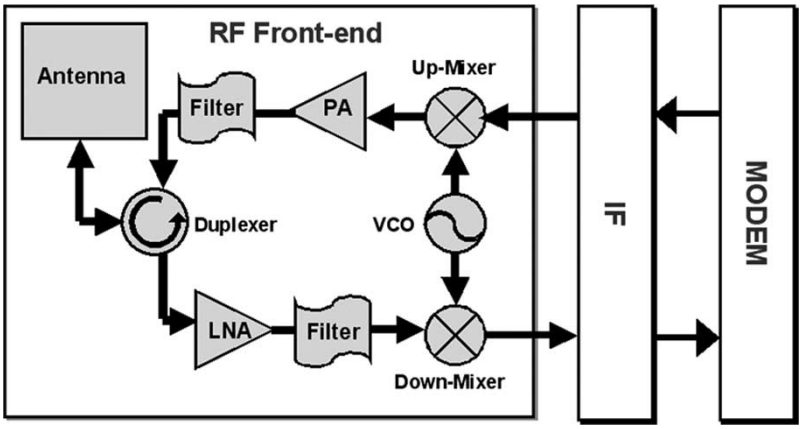


Fig. 12. RF transceiver architecture.

film device with a thickness of $\sim 1\ \mu m$. Each individual PD is picked and inversely bonded onto the host substrates. Thus, the responsivity of the inverted MSM (I-MSM) is improved significantly by eliminating the electrode shadowing effect [41]. The low temperature organic board is pretreated with a planarizing polymer buffer layer and the metal contact pads are sputtered or evaporated on the lower waveguide cladding. The pads are used to either bump-bond with electronic chips or bond directly to the I-MSM-PDs via Van der Waals attraction. Waveguide polymer material is spin-coated directly onto the SOP substrate and photolithographically patterned into the waveguide structure. As shown in Fig. 16, the optical signals propagate along the polymer waveguide and are diffracted by grating couplers to a PD array. Alternatively, the PDs are evanescently coupled to embedded I-MSMs or p-i-n's, as shown in Fig. 17. The evanescent coupling efficiency from the waveguide to a p-i-n is measured to be 3% at 1.3 μm and 1.55 μm [42]. In this way, high speed chip to chip data communication on SOP is realized through the optical devices of photodetectors, waveguides, gratings and other optical components. The bandwidth of the PD/waveguide optical interconnect is primarily dominated by the speed of the photodetector.

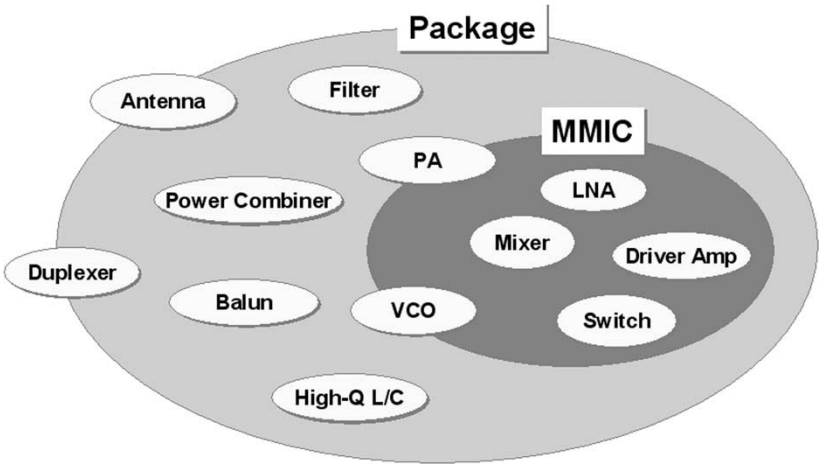


Fig. 13. RF component integration in IC and SOP package.

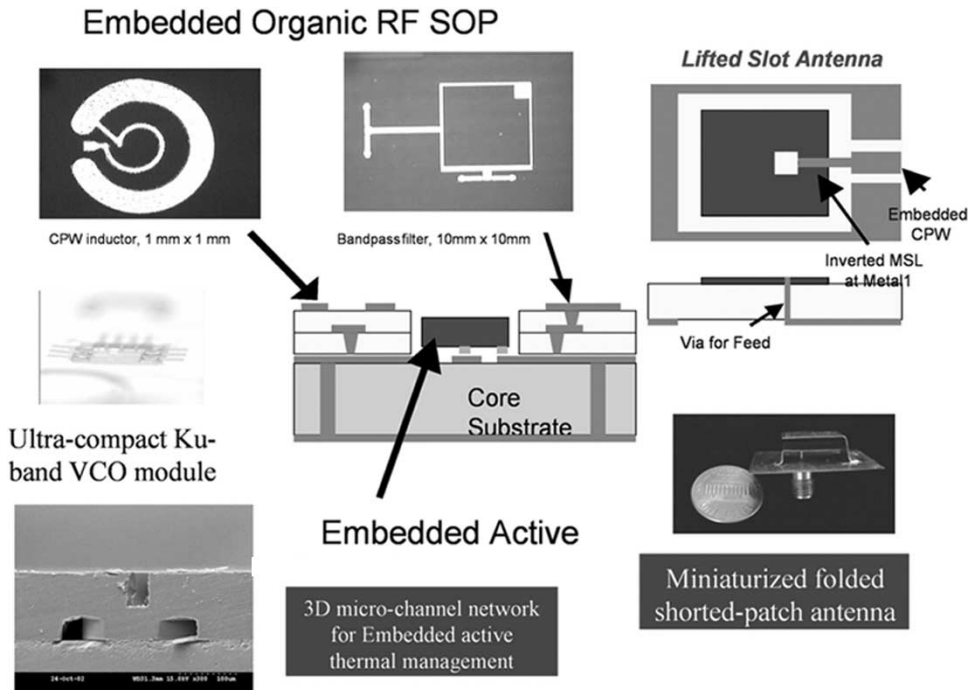
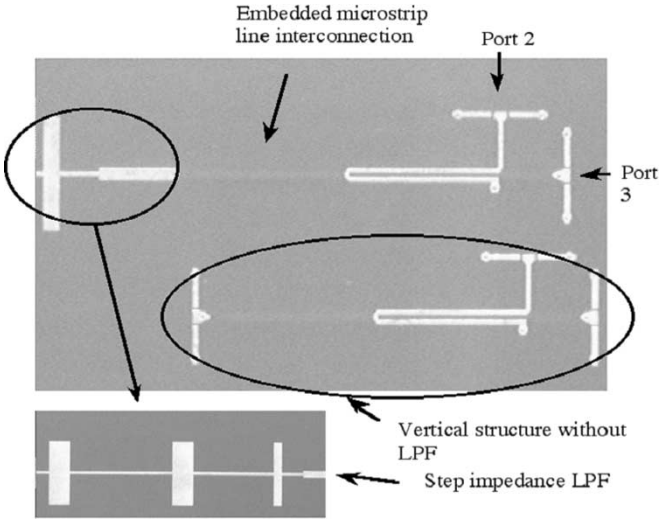


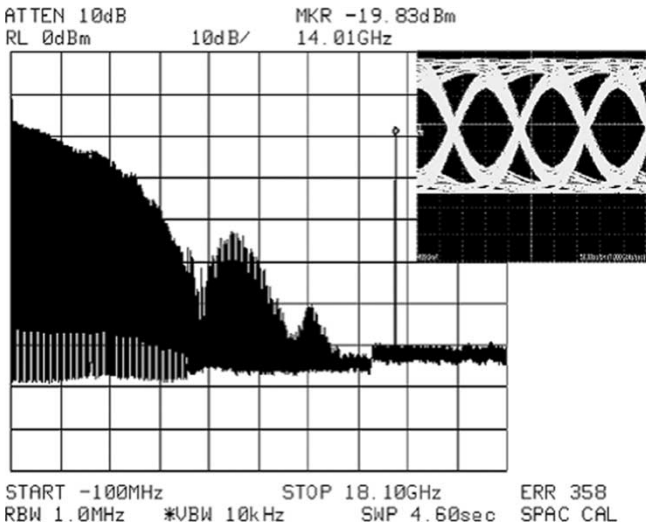
Fig. 14. Components fabricated on organic SOP.

B. Integration of Optical Passives

The primary focus of embedded passives is process and materials for the fabrication of waveguides, gratings, lenses, couplers and switches on low temperature FR-4 boards. The fabrication process itself presents four main issues: 1) Surface roughness of the organic board, 2) interface adhesion, 3) intrinsic and extrinsic waveguide losses, and 4) reliability. Two materials were used in this study: BCB and Siloxane. Suzuki *et al.* [43] reports a surface roughness of $\pm 0.2\ \mu\mathrm{m}$ over a distance of 5000 $\mu\mathrm{m}$ after BCB planarization of a high T_{g} FR-4 board. In another paper in this issue, Chang [42] reports an average surface roughness of 4 nm over 5 $\mu\mathrm{m}$ and $\pm 20\ \mathrm{nm}$ over 500 $\mu\mathrm{m}$ for a low temperature board planarization process. Although few researchers report on interface adhesion, photo-definable Siloxane-based waveguides passed the "Scotch tape" vertical pull test. The optical loss at 1300 nm for BCB waveguides, prepared by RIE, is reported to be 0.36 dB/cm [44], consistent with other reports in the literature. For an Ultem(core)/BCB(cladding) waveguide, prepared by RIE, the reported loss [45], [46] is 1.34 dB/cm at 1330 nm. A photodefinable, epoxy-based Siloxane Oligomer had a measured optical loss of 1.43 dB/cm at the same wavelength [42], and a second photodefinable polymer had a measured loss of 0.2 dB/cm at 1330 nm [42]. Reliability issues such as thermal cycling and accelerated optical aging are seldom reported. An array of 5 waveguides composed of epoxy-based Siloxane Oligomer (Polyzet, Inc., New York) on FR-4 boards were cycled between $-55\ ^{\circ}\mathrm{C}$ and $125^{\circ}\mathrm{C}$. Each waveguide is 5 cm long, and all had a cross section of 50 $\mu\mathrm{m} \times 7\ \mu\mathrm{m}$. After 300 cycles, no measurable change in absorption at the two wavelengths was observed in each of five waveguides in an array. Accelerated optical aging test is ongoing. Fabrication and integration technologies are being developed for micro lenses, micro mirrors, switches and couplers, as well as wavelength pro-



(a)



(b)

Fig. 15. (a) Picture of fabricated combiner in MLO process, 5 mm in length. (b) Frequency spectrum at the output port.

cessing components such as gratings, photonic crystals, arrayed waveguide gratings, multimode interference. Recent global developments in this area can be found elsewhere in this issue [42].

VII. Mixed-Signal SOP Test Research

The PRC research program in mixed-signal test develops electrical functionality validation and performance screening methods for SOP-based systems that include not only high-performance (multigigabits per second) digital signals, but also RF, analog, and optical signals. The research provides cost-effective means to verify functionality and performance in complex "mixed-signal" SOP systems. The Mixed-signal Test research effort is a system level approach that incorporates design-for-test (DFT) and built-in self-test (BIST) features within the SOP design as well as external instrumentation and novel methods for applying tests. To accomplish these, the Systems Test Research involves three areas: 1) design of a high-speed digital test support processor (TSP) for application of multigigahertz tests at the SOP and IC levels [47]–[49]; 2) development of test methods for embedded interconnect and mixed digital/optical signals [48], [49]; and 3) design-for-test methods for Built-In Test of Embedded Mixed-Signal Electronics [50], [51]. The first two research areas share the use of a "Test Support Processor" TSP and are summarized in Section VII-A and the third research area addresses the testing complexities encountered in SOP systems with mixed RF, linear, and digital technologies as outlined below.

A. Test Support Processor for High-Speed Digital and Mixed Digital/Optical Signals

Even though existing digital devices support I/O data rates in excess of 2 Gb/s, current automated test equipment (ATE) is typically limited to speeds of about 1. 0 to 1. 6 Gb/s (per channel). Furthermore, these high-end systems are expensive, costing \$5 k to \$10 k per channel. The capital cost for a fully populated $(\sim 1000\ \mathrm{pin})$ system can be close to \$10 M. Timing accuracy in these systems is also limited to about 50–100 ps, and random jitter is typically 6 ps to 10 ps. Evolution of ATE is extending data rates to 3. 2 Gb/s and above, and optical bit error rate test (BERT) up to 10 Gb/s and above per channel. One of the most difficult barriers to achieving these goals is the extremely precise timing requirement, inherent to testing high-speed signals. Specifically, there is a need to produce much lower-cost, high-speed (multigigahertz) test channels with low jitter $(<2\ \mathrm{ps\ RMS})$ and timing accuracy of 10 to 20 ps. Required bit error rates (BERs) of 10^{-12} require consideration of 14-sigma jitter tolerance. Integration of high-speed optical components, and mixed digital/RF within the low-cost digital embedded test electronics poses significant technical and economic challenges.

To address these testing requirements, the PRC research program has developed the concept of a *Test Support Processor* (TSP). In this approach, the conventional ATE is supplemented with customized electronics that provide specialized test functions tailored for a specific SOP. The prototype designs use a field-programmable gate array (FPGA) and a microcontroller as a "Digital Test Core" (see Fig. 18). The FPGA is reprogrammed to supplement the built-in self test (BIST) features of the SOP. The microcontroller provides a communications port (USB) to a personal computer (which is used to control the testing process). Surrounding the Digital Test Core, is customized high-speed logic that is typically needed to multiplex to higher data rates than can be generated by the FPGA alone. In the example of Fig. 18, this logic is implemented using PECL devices capable of operating to about 5 Gb/s. This example TSP provides multiple 5 Gb/s data sources and receivers for testing nanowafer level packaged IC's. It has been adapted from earlier designs that used the same Digital Test Core. Current efforts are centered on extending beyond 5 Gb/s. In a recent design modification, SiGe logic is used for higher bandwidth and provisions to connect optical transceivers have been added.

VIII. Mixed-Signal SOP Reliability

The mixed-signal reliability research focuses on the reliability of individual digital, optical, and RF functions as well as

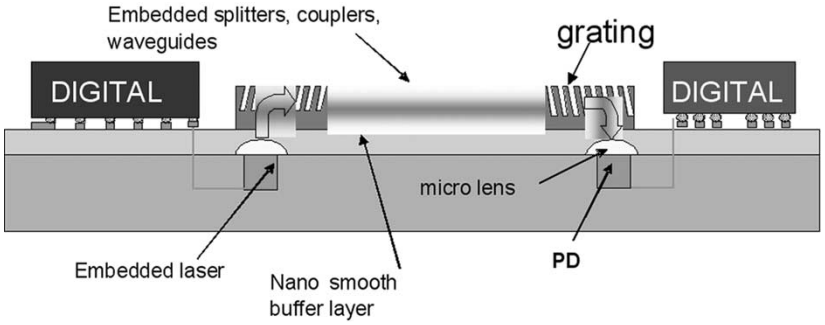


Fig. 16. Optoelectronic SOP chip-to-chip concept and design.

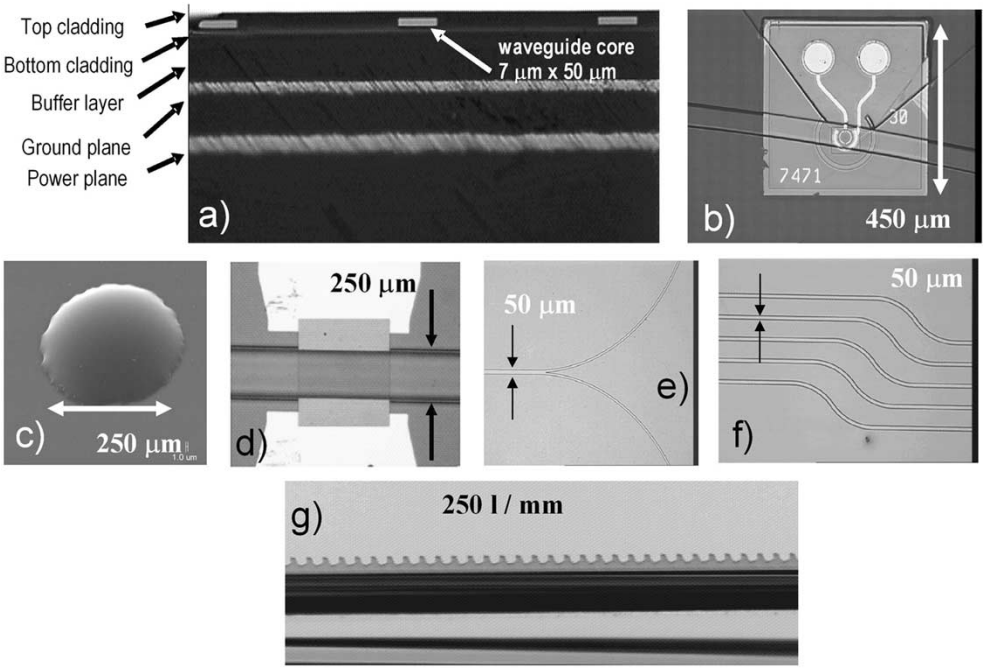


Fig. 17. Optical component technologies embedded in SOP. (a) Waveguide array embedded in FR-4 board, (b) embedded commercial p-i-n detector, (c) polymer microlens, (d) embedded i-MSM, (e) beam splitter, (f) curved waveguide array, (g) blazed polymer grating, blaze angle 29°.

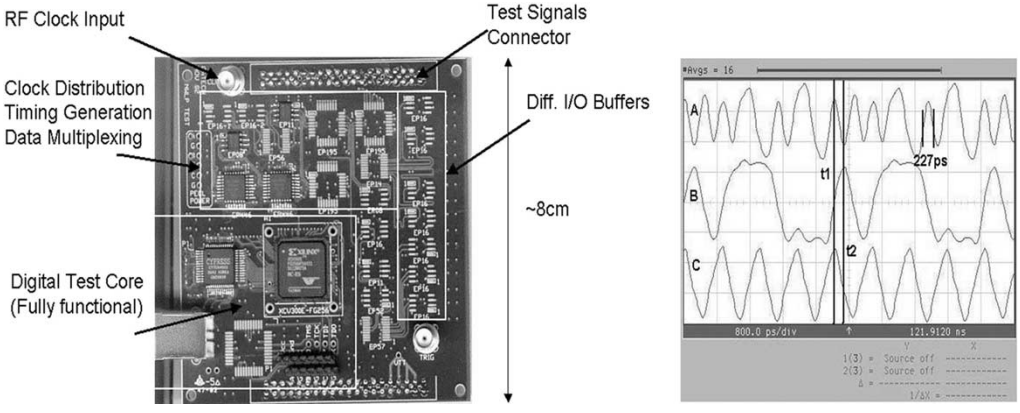


Fig. 18. Test support processor (TSP) prototype, and 4. 4 Gb/s signal output.

the interface between these functions. For digital function reliability, failure mechanisms such as microvia and global interconnect fatigue failure, dielectric cracking and delamination, die-to-substrate solder interconnect fatigue failure, underfill cracking and delamination, etc., are being studied through physics-based predictive models, and the onset of such failure mechanisms is linked to digital function degradation and reliability. Similarly, optical loss in waveguides, refractive index stability, misregistration tolerance, bandwidth limitations as a function of distance, stress-optical effects, and waveguide delamination are being modeled to predict the optical function reliability. Similarly, the changes in inductance, capacitance, and resistance of

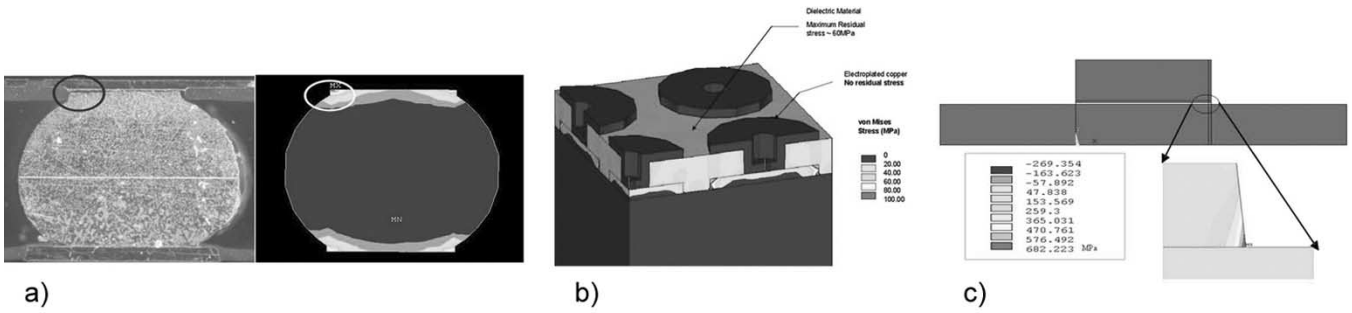
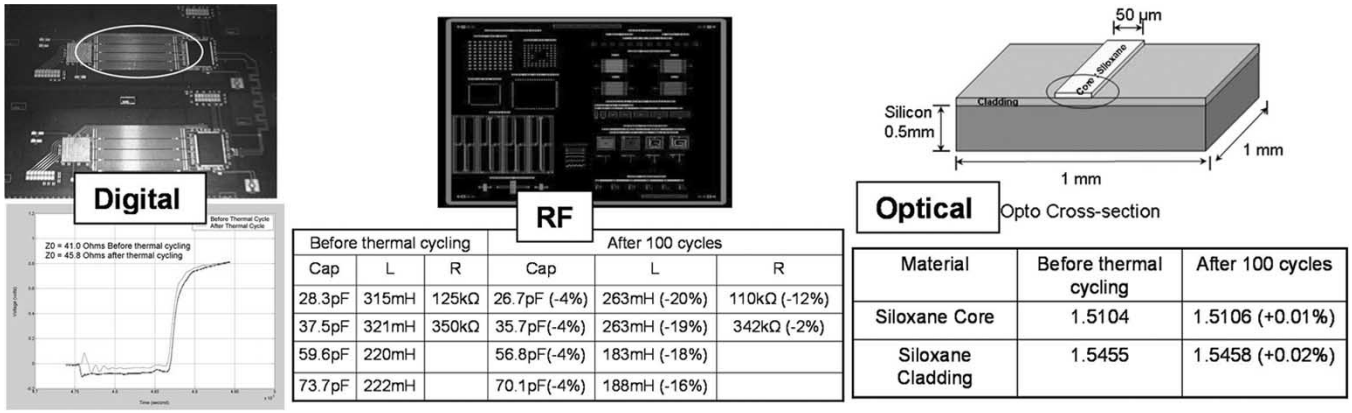


Fig. 19. Reliability prediction models: (a) solder interconnect, (b) microvia, and (c) interlayer delamination.



Before thermal cycling			After 100 cycles		
Cap	L	R	Cap	L	R
28.3pF	315mH	125kΩ	26.7pF (-4%)	263mH (-20%)	110kΩ (-12%)
37.5pF	321mH	350kΩ	35.7pF(-4%)	263mH (-19%)	342kΩ (-2%)
59.6pF	220mH		56.8pF(-4%)	183mH (-18%)	
73.7pF	222mH		70.1pF(-4%)	188mH (-16%)	

Material	Before thermal cycling	After 100 cycles
Siloxane Core	1.5104	1.5106 (+0.01%)
Siloxane Cladding	1.5455	1.5458 (+0.02%)

Fig. 20. Experimental tests to assess individual function reliability.

integral passives with thermal excursions and exposure to environmental conditions are being studied with respect to RF functions. In conjunction with the physics-based models, reliability experiments using individual-function testbeds as well as mixed-signal testbeds are being carried out to validate the models and to enhance the modeling methodologies.

Fig. 19 shows some of the predictive modeling results and Fig. 20 shows some of the experimental data used to validate the predictive models. For more details on the models, experimental reliability tests, and material characterization techniques, please refer to [52]–[61].

In a multi-functional system like in SOP, the digital, optical, and RF functions are inter-related, and therefore, in addition to individual function reliability, the interaction effects should also be studied. For example, 1) the presence of high-performance digital function in proximity to a high flux optical domain could overheat the optical waveguides and affect the waveguide reliability, 2) the processing of low-loss interlayer dielectric to achieve digital function target parameters could adversely affect the reliabiilty of the embedded passive layers fabricated, and 3) the warpage introduced due to the processing of different layers and due to the operation of different functions would adversely affect dielectric reliability, waveguide misregistation and optical fidelity, and passive layer adhesion. Therefore, such interaction effects of various functions are being addressed in the system-level reliability models. Development of such system-level reliability models with multiple functions and failure mode interactions requires tremendous computational resources and time. Innovative modeling techniques augmented with high performance computing are being used to ease the computational complexity and reduce the time needed in achieving acceptable results. In addition, statistical reliability considerations are also being pursued when addressing the system-level reliability.

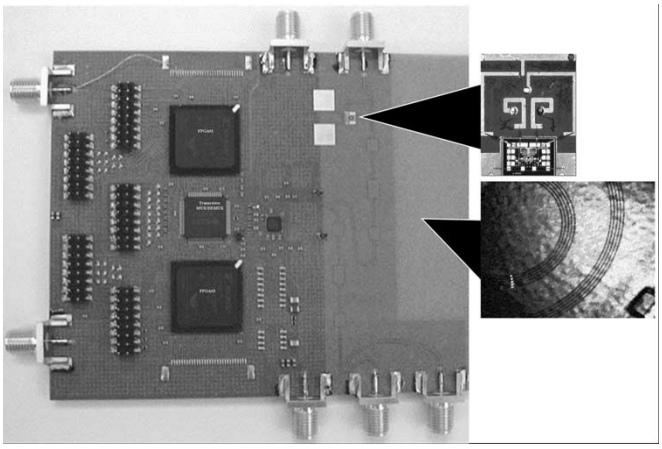


Fig. 21. INC-SOP system fabricated with embedded digital, optical, and RF mixed signal functions.

IX. SOP Technology Demonstration by INC System Prototype

The INC system design and architecture has been successfully fabricated, as shown in Fig. 21 by SOP designs and processes, described above. The prototype system was tested at the each of sub-system blocks such as at RF, digital and opto-electronics. The INC system successfully demonstrated digital

throughput up to 3.6 Gb/s. Optical link data rates in excess of 10 Gb/s, including butt coupling interconnection between optical waveguide and optical fiber. A VCO has been developed and fabricated as part of this INC prototype, using a MESFET process. To reduce the phase noise of the VCO, which is critical in the multi-carrier modulation, the high-Q embedded inductors are built on the SOP package directly. The RF signal generated by VCO with embedded inductor showed $-110\ \mathrm{dBc}$ at 6 MHz offset frequency and $-10\ \mathrm{dBm}$ of output power. After verifying at the sub-system levels, the overall system has been set up on an optical table to prevent unwanted vibration from the embedded optical waveguide interconnection. The demonstration included the signal generated by FPGA combining with RF single carrier signal with optically-modulated signal by MZ modulator. The optical signal was transmitted through the optical fiber and embedded optical waveguide, and then converted into the electrical signals. The system demonstration details can be found elsewhere [62], [63].

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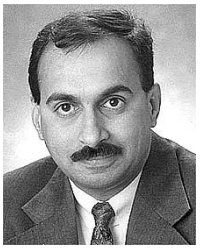

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