

Improved BER Performance of Real-Time DDO-OFDM Systems Using Interleaved Reed–Solomon Codes

Ming Chen, Xin Xiao, Xinying Li, Jianjun Yu, Z. Rena Huang, Fan Li, and Lin Chen

Abstract—In this letter, we have experimentally demonstrated a Reed–Solomon (RS) coded and multiple symbol interleaved real-time orthogonal frequency-division multiplexing (OFDM) signals transmission over a single mode fiber (SMF)-based direct-detection optical system. To the best of our knowledge, this is the first time to realize the forward error correction (FEC) in real-time optical OFDM systems. The bit error rate (BER) performances of RS-coded OFDM signals are investigated in a low-cost directly modulated laser-based direct-detection optical transmission system. The experimental results show that after 25.26-km SMF-28 transmission of the real-time RS-coded and symbol interleaved optical OFDM signals, a post-FEC BER less than 1×10^{-8} is successfully achieved by using RS code with 7% overhead for a pre-FEC BER of 1×10^{-3} .

Index Terms—Optical orthogonal frequency division multiplexing (OOFDM), forward error correction (FEC), Reed–Solomon (RS) coding, intensity-modulated direct-detection (IMDD).

I. INTRODUCTION

OPTICAL orthogonal frequency-division multiplexing (OFDM) has been widely studied by using offline digital signal processing (DSP) approaches, and considered as a promising technology for future broadband access networks and long-haul transmission systems [1]–[3], due to its high spectral efficiency and greater resistance to fiber dispersion. For the offline DSP approaches, the generation and

demodulation of the baseband OFDM signal are realized by offline programs without fully considering the complexity of hardware implementation. To further investigate the feasibility of OOFDM technology, the base-band OFDM transceiver should be implemented with the help of real-time digital signal processing (DSP) algorithms in the field programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs). Only by this way, the off-line DSP algorithms can be truly verified for real applications in the future. So far, some real-time OFDM transmitters and/or receivers have been experimentally demonstrated in both direct-detection and coherent optical fiber transmission systems [4]–[10]. In [4], a 30-Gb/s real-time triple-band direct-detection optical OFDM (DDO-OFDM) system was demonstrated in a passive optical network (PON). The transmission and reception of 100 Gb/s polarization multiplexed OOFDM signals over several hundreds of single mode fibers (SMFs) have been experimentally demonstrated in coherent optical systems [8], [9]. More recently, real-time reception of 256.5 Gb/s four-channel wavelength-division multiplexed OFDM signal has been demonstrated in 2.4-km SMF DDO-OFDM system [11]. In addition to OOFDM, demonstration of real-time 40 Gb/s pulse amplitude modulation with four amplitude levels (PAM-4) for next generation access applications was also reported in [12]. However, the bit error rate (BER) performance is always limited by various non-linearity effects and noises of optical systems. Without using forward error correction (FEC) technique, the BERs in these real-time systems are too high to meet the requirement in practical applications. To improve BER performance as well as receiver sensitivity, one of the key approaches is to apply powerful forward error correction (FEC) technique.

It is well known that Reed–Solomon (RS) coding has a strong ability to correct both burst errors and random errors, and has been widely used in wireless and fiber-optic systems [13]. The non-perfect frequency responses of the electrical and optical components, for example, the roll-off effect of digital-to-analog converters (DACs) can cause large power attenuation to the high-frequency subcarriers, high BERs will occur on these subcarriers with low signal-to-noise ratios (SNRs). As a result, the performance of the corresponding RS decoder may be degraded. Usually, the symbol interleaving is necessary after RS encoder to achieve improved error correcting capability in the receiver. In [14], an improved RS coding based on power loading and bit-interleaving for DDO-OFDM is studied by offline approaches. It shows that, the BER performance can be significantly improved by using RS codes. As far as we know, in addition to RS code, many

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M. Chen is with the Department of Electrical, Computer, and System Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180 USA, also with ZTE TX Inc., Morristown, NJ 07960 USA, and also with the College of Physics and Information Science, Hunan Normal University, Changsha 410081, China (e-mail: cm_ccsu@126.com).

X. Xiao and F. Li are with ZTE TX Inc., Morristown, NJ 07960 USA (e-mail: xiao.xin@ztetx.com; fanli0809@gmail.com).

X. Li and J. Yu are with the Key Laboratory for Information Science of Electromagnetic Waves, Ministry of Education, Fudan University, Shanghai 200334, China (e-mail: smileseaxy@gmail.com; jianjun@fudan.edu.cn).

Z. R. Huang is with the Department of Electrical, Computer, and System Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180 USA (e-mail: huangz3@rpi.edu).

L. Chen is with the Key Laboratory for Micro/Nano Optoelectronic Devices, Ministry of Education, College of Computer Science and Electronic Engineering, Hunan University, Changsha 410082, China (e-mail: liliuchen12@vip.163.com).

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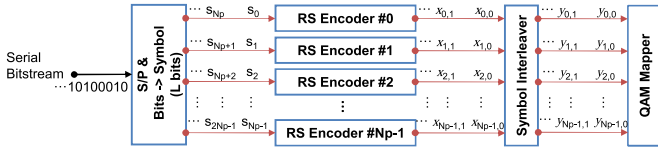


Fig. 1. Block diagram of RS encoding and multiple-symbol interleaving scheme.

research efforts have been done on other advanced codes (e.g., Turbo codes, low-density parity-check (LDPC) codes) for optical OFDM by offline DSP approaches [15], [16].

In this letter, to the best of our knowledge, we experimentally demonstrate a real-time RS coded and multiple-symbol interleaved (IL) FEC technology in DDO-OFDM system for the first time. The BER performances of the RS (288, 256), RS (274, 256) and RS (1023, 955) encoded, and 16-ary quadrature amplitude modulation (QAM) real-time OFDM signals are investigated in a directly modulated laser (DML) and SMF-based DDO-OFDM transmission system.

II. ENCODING AND SYMBOL-INTERLEAVING SCHEME

High-speed fiber-optic communications often work at data rates of several gigabits per second or even more. Today, even the state-of-the-art FPGA can only be clocked at a few hundred megahertz. To fully process the received samples, it is necessary to implement the parallel DSP structures in FPGAs. By doing so, the FPGAs can work at a lower clock frequency to meet the timing constraints. Usually, due to the imperfect frequency response in the optical and electrical devices such as roll-off effect of DAC, and other interferences such as subcarrier-to-subcarrier intermixing interference (SSII) [17], most of the error symbols are located on the subcarriers (SCs) with low SNRs. To avoid excessive error symbols being assigned to a certain RS decoder, which would cause a decoding failure, a simple multiple-symbol interleaving and de-interleaving scheme is proposed to disorder the distribution of error symbols.

The RS encoding and interleaving scheme for the real-time transmitter is illustrated in Fig. 1. First, the high-speed serial bit-streams are converted to $N_p \times L$ parallel bits, where N_p is the number of the parallel encoders, and L is the number of bits per symbol ($s_0, s_1, s_2, \dots, s_{N_p-1}$). Then, $N_p \times L$ parallel bits are fed into N_p RS encoders simultaneously at the rising edge of FPGA clock. The N_p encoded symbols ($x_{0,n}, x_{1,n}, x_{2,n}, \dots, x_{N_p-1,n}$) in the n -th FPGA clock period are sent to the interleaver to reorder the input symbols, and the relation between the reordered symbols ($y_{0,n}, y_{1,n}, y_{2,n}, \dots, y_{N_p-1,n}$) and inputted symbols can be expressed as

$$y_{m,n} = x_{(m+n) \bmod N_p, n} \quad (1)$$

where m is the index of RS encoder with a range of $[0, N_p-1]$, and \bmod is the modulo operation. For each OFDM symbol generation, an integer multiple of N_p RS-encoded and interleaved symbols regarded as a block will be fed into the QAM mapper, which outputs N_{SC} QAM-mapped symbols. Here, N_{SC} is the number of data-carrying SCs of an OFDM symbol. Subsequently, the QAM mapped symbols will be modulated on the corresponding SCs by inverse fast Fourier transform (IFFT) operation. For example, the modulation

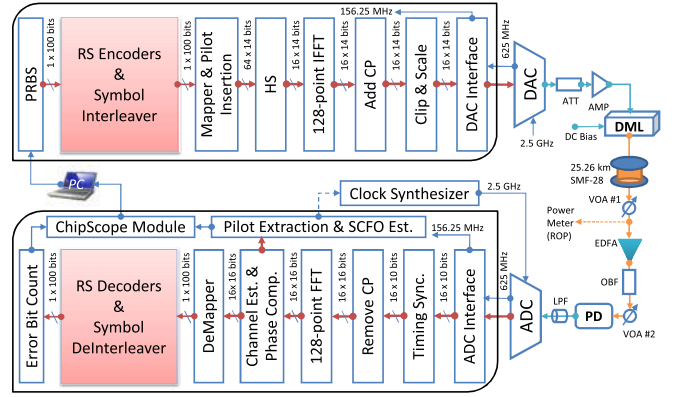


Fig. 2. Experimental setup for the RS coded and symbol interleaved real-time DDO-OFDM system.

format is 16-QAM, N_{SC} is 50, and both L and N_p are 10, two continuous N_p RS-encoded and interleaved symbols ($y_{0,n}, y_{1,n}, y_{2,n}, \dots, y_{N_p-1,n}, y_{0,n+1}, y_{1,n+1}, y_{2,n+1}, \dots, y_{N_p-1,n+1}$) with a total of 200 bits outputted from N_p parallel RS encoders, are 16-QAM mapped, and then modulated on 50 data-carrying SCs.

The reverse scheme is applied for RS decoding and symbol de-interleaving. After symbol de-interleaving, error symbols on these SCs with low SNRs can be evenly distributed to every RS decoder. Therefore, the decoding failure which is caused by the excessive error symbols assigned to one RS decoder can be, to some extent, avoided.

III. EXPERIMENTAL SETUP AND DSP IN REAL-TIME BASE-BAND TRANSCIVER

The experimental setup for the RS coded and symbol interleaved real-time DDO-OFDM system is shown in Fig. 2. More details of the FPGA-based real-time DSP algorithms in the OFDM transceiver could be found in [18] and [19]. The off-line generated pseudo-random binary sequence (PRBS) is stored in the read only memory (ROM) on transmitter FPGA. The DSP algorithms in the transmitter include RS encoding, multiple-symbol interleaving, QAM mapping, pilot insertion, Hermitian symmetry (HS), IFFT, cyclic prefix (CP) addition, clip and scale, and DAC interface function. For RS encoder, both L and N_p are set to 10. The proposed RS coding scheme can be easily scaled by only adding more parallel RS encoders/decoders to support higher speed OOFDM systems with a data rate of 40 Gb/s and beyond. Three RS codes, RS (274, 256), RS (288, 256) and RS (1023, 955), are implemented in the transceiver. The size of IFFT is 128. Only 50 positive SCs are used to carry QPSK 16-QAM-encoded complex symbols. 4 pilot SCs are modulated by BPSK symbols for sampling clock frequency offset (SCFO) estimation. DC SC, 9 positive high-frequency SCs and Nyquist SC are filled with zeros. To create a real OFDM signal, 63 negative-frequency SCs are the complex conjugates of the 63 corresponding positive-frequency SCs. After IFFT process, a 16-point CP is employed. The digital OFDM signal is clipped at a clipping ratio of 11.5 dB. The clipped signal is then scaled and sent to 14-bit DAC operating at a sample rate of 2.5 GS/s via DAC interface, which also provides a clock of 156.25 MHz for the transmitter FPGA. Here, an OFDM frame consists of a random 512-point bipolar non-return-to-zero

TABLE I
PARAMETERS OF THREE FEC SCHEMES

FEC Scheme	OH	FPGA Resources		Latency	
		LUTs/FFs/Block RAMs*		(Clock Cycles)	
		ENC**	DEC	ENC	DEC
RS (274, 256)	7.03%	332/195/0	1271/903/1	3	527
RS (288, 256)	12.5%	558/335/0	2001/1477/1	3	954
RS(1023, 955)	7.12%	1040/696/0	3470/2207/2	3	3651

* LUT: look-up-table, FF: flip flop pairs, RAM: random access memory.

** ENC/DEC: encoder/decoder

encoded pattern for symbol timing synchronization, 4 training sequences (TSs) for channel estimation, and followed by 256, 274, 288 and 288 data-carrying OFDM symbols for without FEC, RS (274, 256), RS (288, 256) and RS (1023, 955) coding cases, respectively. For the RS (1023, 955) coded system, the net rate is 3.14 Gb/s after excluding the overheads (OHs) of CP, pilot symbols, symbol timing synchronization pattern and FEC. The OHs, required FPGA resources and latency for each FEC scheme are listed in Table I. It should be mentioned that the required FPGA resources are only for each RS encoder or decoder.

The DAC generates an analog OFDM signal with a peak-to-peak voltage (V_{pp}) of ~ 600 mV. First, the signal is attenuated, then amplified by a linear RF amplifier (AMP) up to ~ 2.5 Vpp, together with an optimum DC bias current of 44 mA, and then injected into a 1558.17 nm directly modulated laser (DML) with a 3 dB modulation bandwidth of ~ 10 GHz. The intensity-modulated optical OFDM signal with a power of 4.3 dBm is coupled into the 25.26 km SMF-28 fiber. At the receiver, the first variable optical attenuator (VOA #1) is used to obtain OOFDM signal with different received optical powers (ROPs). After passing through the VOA #1, the attenuated signal is pre-amplified by an erbium-doped fiber amplifier (EDFA) with a noise figure of 5 dB, followed by an optical band-pass filter (OBF) with a bandwidth of ~ 0.9 nm. Here, the EDFA as a pre-amplifier can be used in the receiver of optical line terminal (OLT) for upstream link, and shared by all optical network units (ONUs) [12]. To balance ADC quantization noise and clipping noise induced by the 10-bit ADC, the optimum input power for the photo-detector (PD) is required to maintain at 2 dBm. So the amplified OOFDM signal is attenuated by the second VOA (VOA #2). The attenuated OOFDM signal is directly detected by a 10 GHz PD, and then passes through an electrical low-pass filter (LPF). The 2.5 GS/s digital samples incorporating with a 625 MHz clock are fed into receiver FPGA via ADC interface, which provides a 156.25 MHz operating clock for the receiver FPGA. It should be noted that 16-parallel channels DSP structure is implemented in both baseband transmitter and receiver FPGAs, which operate at 156.25 MHz is to achieve 2.5 GS/s samples for the DAC and ADC. The receiver DSP functions include symbol timing synchronization, CP removal, FFT, channel estimation and phase compensation, de-mapping, symbol de-interleaving, RS decoding and error bit count. In addition, the pilot-aided SCFO estimation is also performed for sampling clock frequency synchronization between the DAC and ADC. The number of error bits, TS-based channel response estimation, only phase-compensated 16-QAM complex symbols and ADC captured samples for SNR estimation [20] are uploaded

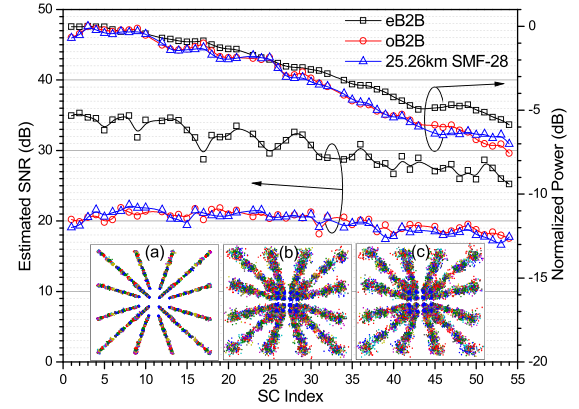


Fig. 3. Estimated SNR and frequency response v.s. SC index. Insets (a), (b) and (c) are the only phase-compensated 16-QAM constellations for (a) eB2B; (b) oB2B; (c) after 25.26 km SMF-28 transmission at -25 dBm ROP.

into a host PC by ChipScope module. The sampling clock synchronization is achieved by manually adjusting the output of a clock synthesizer according to the estimated SCFO at the initial stage.

IV. RESULTS AND DISCUSSIONS

The real-time estimated frequency responses and off-line estimated SNRs from received OFDM samples for three cases as electrical back-to-back (eB2B), optical back-to-back (oB2B) and 25.26 km SMF-28 transmission, are shown in Fig. 3, respectively. There is about 6 dB power attenuation on the highest data-carrying SC. It is mainly due to the roll-off effect of the DAC and limited bandwidth of analog front-ends of DAC and ADC. The imperfect frequency responses of optical components result in additional up to 2 dB power attenuation on the high-frequency SCs for both oB2B and SMF transmission compared with eB2B. For SNR estimation, the estimated SNRs for both oB2B and SMF transmission are rapidly degraded compared with eB2B, which is mainly attributed to the ASE noise of the EDFA. The only phase-compensated 16-QAM constellations for eB2B, oB2B and after SMF transmission (ROP = -25 dBm) are also given in Figs. 3(a), (b) and (c), respectively.

To explore the transmission performance of our RS coded and symbol interleaved real-time DDO-OFDM system, the real-time OFDM signals transmission over 25.26 km SMF-28 system is experimentally investigated. The error bits in continuous 2048 OFDM frames with a total of more than 100,000,000 information bits are counted for BER measurement. The real-time measured BER versus ROP is plotted in Fig. 4. It can be seen that the RS coded and symbol interleaved systems have better BER performance than only RS coded systems. Compared to the RS (274, 256) coded system, the RS (1023, 955) coded system has similar FEC overhead, but has better BER performance at the expenses of more FPGA resources and higher latency. At a pre-FEC BER of 1×10^{-3} , a post-FEC BER less than 1×10^{-8} is successfully achieved by using RS (1023, 955) or RS (288, 256) code. Here, the BER values for RS (288, 256) with IL, RS (1023, 955) with IL, RS (274, 256) with IL, RS (288, 256) only, and RS (274, 256) only at an ROP higher than -31 , -29 , -28 and -26 dBm, respectively, are zeros. It should be mentioned that, error free

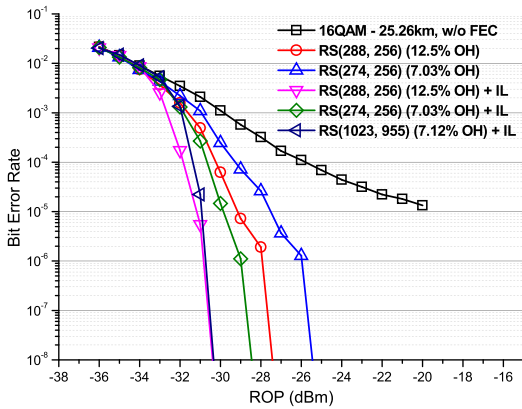


Fig. 4. Real-time measured BER v.s. ROP for 16-QAM-encoded DDO-OFDM system.

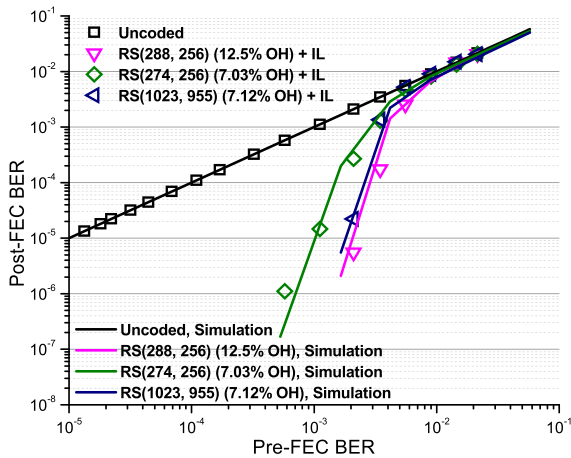


Fig. 5. BER performance comparison between experiment and simulation.

at the above mentioned ROPs are observed for more than one hour real-time BER measurements. So we believe that a post-FEC BER below 1×10^{-9} can be reached at a pre-FEC BER of 1×10^{-3} when RS (288, 256) with IL or RS (1023, 955) with IL is used. Thus, the coding gain is more than 10 dB in terms of ROP at the post-BER of 1×10^{-9} as shown in Fig. 4.

To evaluate the decoded BER performance in our real-time system, numerical simulations are performed in an ideal additive white Gaussian noise channel. The parameters for OFDM signals and DSP algorithms in the transceiver are the same as those of the experiment. The experimental results well agree with the simulation ones as plotted in Fig. 5. Here, the pre-FEC BER is equal to uncoded BER.

V. CONCLUSION

In this letter, we have experimentally demonstrated the generation, transmission and reception of real-time RS coded and multiple-symbol interleaved OOFDM signals for the first time. After 25.26 km SMF-28 transmission, at a pre-FEC BER of 1×10^{-3} , the post-FEC BER below 1×10^{-8} was successfully achieved by using 7% overhead RS (1023, 955) code and the simple multiple-symbol interleaving/de-interleaving scheme. The results exhibit that

the multiple-symbol interleaving scheme can significantly improve BER performance as well as receiver sensitivity.

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