Silicon Electro-Optic Modulators Using Quantum Tunneling Structures

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***Abstract*—Injection-type silicon electro-optic modulators are widely used in onchip optical interconnections due to its high modulation efficiency. However, as the modulator dimension approaches the wavelength limit, it becomes hard to improve the modulator speed by shrinking the device. A new approach to further scale down the dimension of an intrinsic device in injection-type electro-optic modulators without suffering from subwavelength confinement problem is proposed. The device consists of stacked PN or PiN cells connected by tunneling structures to enable current conduction. The diffusion capacitance is reduced due to the reduction of quasi-neutral region width in each device. In this paper, a detail study is given to the case of a two-cell modulator. A twofold of capacitance reduction and speed improvement are observed. Further speed improvement is expected by splitting the modulator into more cells, and the simulation approach for the tunneling structures in such an optical device is also discussed in details.**

***Index Terms*—Electro-optic modulation, intensity modulation, optical interconnections, photonic integrated circuits.**

I. Introduction

With the continuous scaling of the CMOS technology, interconnects within a silicon chip becomes more of an obstacle for performance improvement due to large *RC* time delay and crosstalk. Optical interconnects is now widely accepted as a viable solution to provide next generation of high performance computing electronics for applications in data centers or high-end severs [1]. As a key part of the optical interconnects on silicon chips, electro-optic (EO) modulators have been made great progress in recent years and attracted many interests [2]–[6]. Two types of EO modulators based on the free carrier plasma effect were developed in the past decade: one is an injection type modulator that enables carrier injection to manipulate the optical refractive index [3]–[5]; the other one is a depletion type modulator that alters the refractive index of the silicon waveguide by changing the width of the space charge region of a PN junction [2], [6]. A depletion type of modulator has intrinsically high operation bandwidth but low modulation efficiency due to limited carrier density change, typically less than 1×10^{18} cm^{-3} [2], [6]. An injection type of modulator usually has much higher carrier density change ($>1 \times 10^{18}$ cm^{-3}), thus producing better modulation efficiency [3], [5]. Smaller footprint of EO modulators is always on demand because the surface area of a silicon chip is finite. The fastest injection type EO modulator ever reported, which utilizes PiN structure, has a bandwidth of a few gilbert per seconds [3]. When the PiN EO modulator is incorporated in a ring resonator structure, the bandwidth was expanded to 18 Gbps [4]. The drawback of a resonator structure is the reduced optical spectrum width, as well as intolerance to fabrication errors and temperature fluctuation. The goal of this work is to introduce a new design to boost the operation speed of a typical injection type of Si EO modulators.

A silicon EO modulator usually incorporates a rib waveguide structure in the device [2]. The electrical configuration of the rib waveguide may utilize PN, PiN, metal–oxide–semiconductor capacitor or heterojunction bipolar transistor (HBT) [2]–[6]. Junction capacitance is the dominant source of the *RC* time delay for depletion type of Si EO modulators, while the diffusion capacitance is the main source for injection type of EO modulators. Both junction capacitance and diffusion capacitance can be reduced by scaling down the cross section of the junction, which is the common approach to improve the speed of EO modulators in recent years. In addition, the reduction of the device dimension along the current flow direction also helps to reduce the diffusion capacitance.

As the size of the modulator approaches the optical signal wavelength, i.e., $\sim$450 nm in silicon (1.55 μm in air), further scaling of the modulator to sub-wavelength regime will lead to poor confinement of the optical mode [7]–[9]. This is the underline reason for lacking of speed improvement in the past several years. In this paper, a new approach, namely multi-cell PiN and PN structures connected by tunneling structure is proposed to enable further scaling of the dimension along current flow direction for injection type modulators to improve the speed.

II. Modulator Design

Injection type modulators usually are a PN or PiN diode switching between forward bias and thermal equilibrium state to represent the two digital states for data communication, as shown in Fig. 1(a). To maintain optical mode confinement, the typical dimension of the diode is on the order of 300 to 500 nm [2]–[6].

Both junction capacitance and diffusion capacitance cause *RC* time delay for the device performance. In this part, the notation of "capacitance" refers to the unit area capacitance following the convention of most semiconductor literatures. The junction capacitance (C_j) arises from the change of the depletion region

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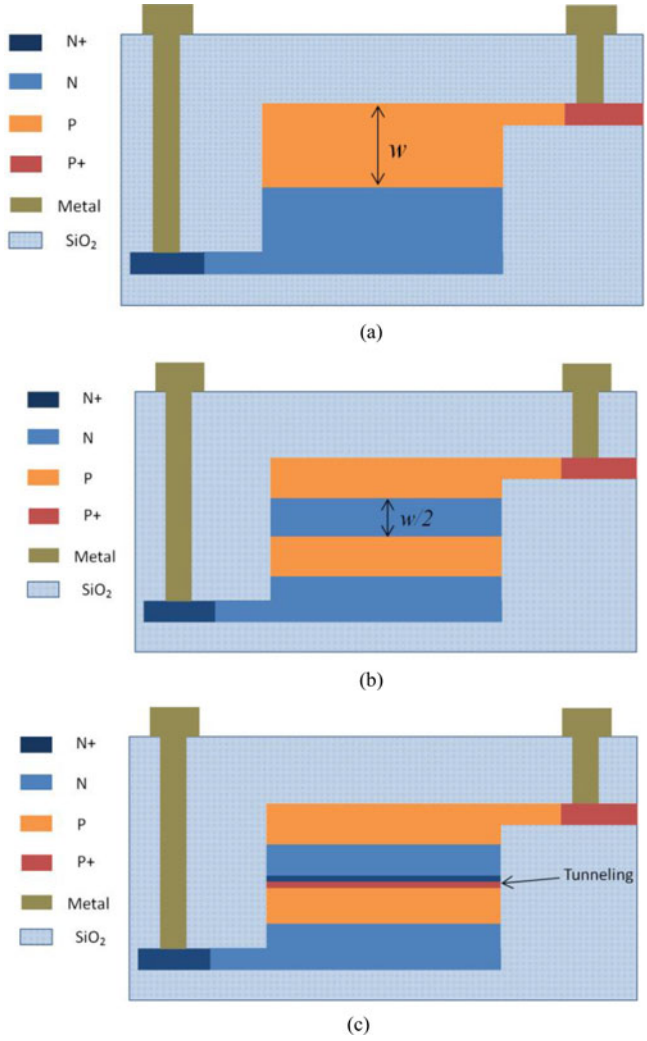

Fig. 1. Schemetics of the cross-section of injection type EO modulators. (a) Conventional design. (b) Stacking PN jucntions in one modulator. (c) Connecting PN junctions by tunneling structures in one modulator.

width (Δw_d) and can be calculated by

$$C_j = \frac{\varepsilon_{\rm Si}}{w_d} = \sqrt{\frac{\varepsilon_{\rm Si} q N_A N_D}{2(N_A + N_D)(V_{bi} - V_A)}} \tag{1}$$

where w_d is the width of depletion region, N_A is the doping level in *P* region, N_D is the doping level in *N* region, V_{bi} is the built-in voltage and V_A is the applied voltage across the junction. The diffusion capacitance is due to the concentration fluctuation of the excess minority charges (ΔQ) in the quasi-neutral region. The excess minority carriers increase exponentially with the forward bias voltage and are the primary source of the capacitance under forward bias. The diffusion capacitance (C_d) is given by

$$C_d = \frac{dQ}{dV_A} = \frac{d\left(\int_0^w qn_p(x)dx + \int_0^w qp_n(x)dx\right)}{dV_A} \tag{2}$$

where w is the width of the quasi-neutral region, $n_p(x)$ is the injected electron concentration in *P* region and $p_n(x)$ is the injected hole concentration in *N* region.

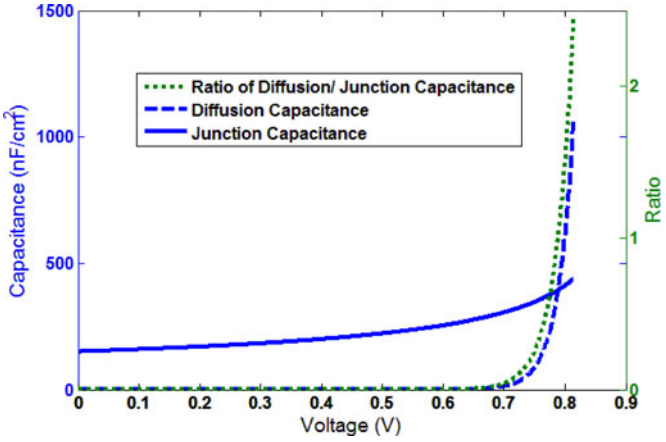

Fig. 2. Capacitance under forward bias in a symmetrically doped PN junction (Doping level 5×10^{17} cm^{-3} and quasi-neutral region width $w = 200$ nm).

The choice of doping affects the capacitance of the device as well as the optical propagation loss. To keep the propagation loss in a reasonable range, a doping less than 1×10^{18} cm^{-3} is often chosen [3]. In our earlier publication, a detailed discussion on optical loss verse carrier concentration was presented [5]. In this work, we calculated the junction capacitance and diffusion capacitance with the forward bias voltage. The width of the *P* and *N* region, i.e., *w* in Fig. 1(a) is kept as 200 nm in the calculation. The capacitances calculated from in (1) and (2) were performed by MATLAB and the result is shown in Fig. 2. The total capacitance is the sum of C_j and C_d. We also used drift-diffusion based ac small signal simulation by Sentaurus to calculate the capacitance of the device and obtained a result that differs by 10% from the MATLAB calculation. At low forward bias voltage, C_j is dominant because there is only a small number of minority carriers injected into the junction. According to our calculation, at approximately 0.78 V for the device shown in Fig. 1(a), C_d surpasses C_j and increases with bias voltage exponentially. For most injection type of EO modulator, the typical forward bias voltage for "ON" status is much higher than 0.8 V, for example, 1.1 V for an HBT EO modulator [5], 1.8 V for a PiN type of EO modulator [3], and 2 V for PiN based ring resonator [4]. Therefore the diffusion capacitance (C_d) plays the key role in determining the speed of injection type EO modulators. It is essential to reduce C_d in order to suppress the *RC* time delay of the injection type of silicon EO modulator.

When the diffusion length is much larger than the quasi-neutral region width *w*, the minority carrier distribution varies near linearly with distance and C_d can be simplified as

$$C_d = \frac{dQ}{dV} = \frac{wq^2 n_i^2}{N_D kT} \exp\left(\frac{qV}{kT}\right) \tag{3}$$

where *w* is the width of the quasi-neutral region and N_D is the doping level in the quasi-neutral region if both sides are doped at the same level. Here n_i is the intrinsic carrier concentration level in silicon. The diffusion length of minority carriers in silicon is typically on the order of micrometers [10] and the dimension of PN or PiN Si EO modulator is in the range of 300

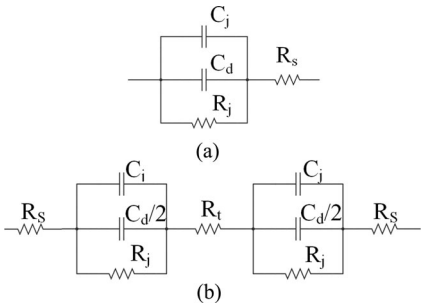

Fig. 3. Equivalent circuit models. (a) PN modulator. (b) PN modulator with tunneling structures.

to 500 nm. So the assumption for this simplification is solid for most Si EO modulators. It can be seen from (3) that one possible approach to reduce C_d is to reduce w by splitting one PN or PiN unit into multiple cells. A sketch of such a device is shown in Fig. 1(b). The quasi-neutral region width w_s of each PN cell is reduced approximately by half. If the modulator is split into more cells, C_d can be reduced further. However, current flow is needed to function as an injection type of Si EO modulator. The device configuration (NPNP) in Fig. 1(b) doesn't conduct current because the P region of cell 1 and N region of cell 2 forms a reversed biased junction. These kinds of structures are similar to thyristor structures and it will not turn on without the assistant of an extra gate terminal.

One solution to enable current flow in a thyristor-like structure is to incorporate a tunneling structure between two adjacent PN or PiN cells. As shown schematically in Fig. 1(c), a heavily doped thin layer of P is added to cell 1 while a heavily doped N layer is added to cell 2. These two layers enable band-to-band tunneling under small reverse bias voltage. The doping levels of the tunneling structures are usually higher than 1×10^{20} cm^{-3} while the thickness of each layer is kept thin to reduce optical loss. The tunneling structure also supplies carriers for injection since the band-to-band tunneling functions as carrier generation centers. The equivalent circuit models for structures in Fig. 1(a) and (c) are shown in Fig. 3. The tunneling layers are represented by a resistor R_t in the model. The total capacitance is reduced by at least a factor of *N*, where *N* is the number of cells of one modulator device. The total resistance increases by a value of R_t, which plays an important role in determining whether speed can be improved or not. In summary, the structure proposed in Fig. 1(c) can switch ON and OFF like a PiN and at the same time reduces the diffusion capacitance without shrinking the total size of the modulator.

III. Numerical Modeling of Tunneling EO Modulators

In the above discussion, a PN junction modulator is used as an example to explain how tunneling structures are incorporated in the new proposed modulator. In practice, most injection type of modulators is based on PiN structure to achieve large modulation efficiency. In the following discussion, the electrical structure of the device is PiN like, i.e., a $P^+N^-N^+$ structure. The geometry of the device is kept as a rib waveguide as sketched in Fig. 4(a).

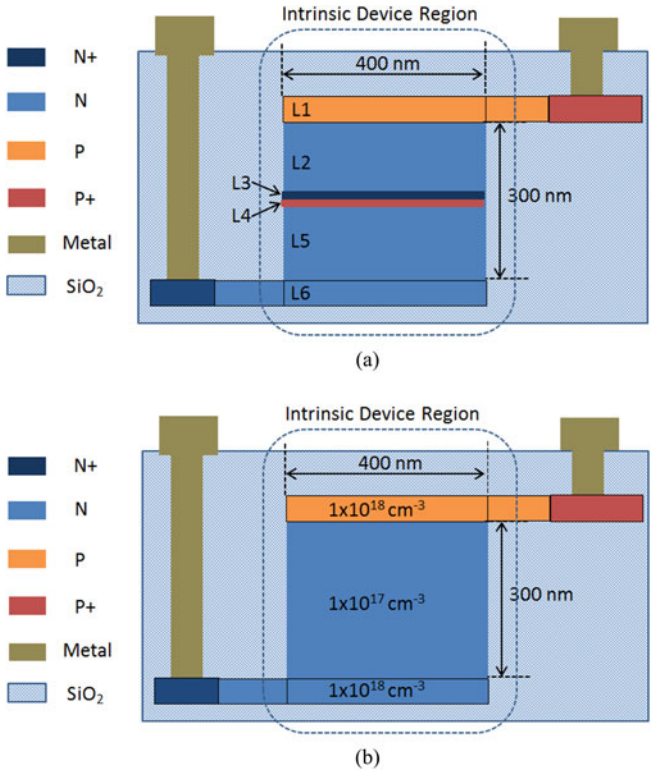

Fig. 4. (a) Structure of the proposed tunneling modulator. (b) Conventional PiN modulator structure.

TABLE I
Layer Structure of Proposed Tunneling Modulator

Layer #	Doping type	Doping level	Thickness
L1	P	1×10^{18} cm^{-3}	50 nm
L2	N	1×10^{17} cm^{-3}	140 nm
L3	N^+	1×10^{20} cm^{-3}	10 nm
L4	P^+	1×10^{20} cm^{-3}	10 nm
L5	N	1×10^{17} cm^{-3}	140 nm
L6	N	1×10^{18} cm^{-3}	50 nm

The thickness and doping of each layer of a two-cell modulator is listed in Table I. Fig. 4(b) shows a conventional PiN modulator structure that has exactly the same dimensions, which is used for comparison in the following discussions.

The proposed tunneling modulator structure can be fabricated by silicon epitaxial growth with *in-situ* doping technology. First, ion implantation is used on a starting wafer to form the bottom contacting layer. Next, six layers of doped silicon are grown by ultra-high-vacuum chemical vapor deposition or low pressure chemical vapor deposition with thickness according to Table I. These six layers are doped during the epitaxial growth process by mixing boron and phosphorus gas with silicon precursors. The process is very similar to the delta-doping technology used in III–V semiconductor [11]. The minimum layer thickness is determined by how fast each dopant gas can be removed from chamber as well as the silicon growth rate. Carbon can be added during the epitaxial growth to reduce the diffusivity of dopants.

A layer of 10 nm thicknesses is feasible for nowadays growth technology. After epitaxial growth, the wafer needs to be patterned through photolithography and etched properly to form the rib waveguide region. The following step is to cover the device with SiO_2. Finally, the top contacting layers are formed by a non-selective crystalline silicon epitaxial growth or polysilicon deposition.

A 2-D simulation by Sentaurus was used to study the electrical characteristics of the proposed Si tunneling EO modulator. The simulation is based on classical drift-diffusion method, and other physics models like Slootboom bandgap narrowing model, Shockley-Read-Hall, Auger recombination model and Philips unified mobility model were also included. The depth of the device, i.e., the length in optical wave traveling direction is assumed to be 1 μm. Thus, all the device parameters discussed below are normalized to 1 μm.

The tunneling structures between adjacent cells are the key parts in the modeling. There are two types of band-to-band tunneling in silicon [12]: phonon assisted indirect tunneling and trap-assisted tunneling. Trap-assisted tunneling is affected by the density of traps as well as the position of the traps in the energy bandgap, so can vary greatly from one process to another. Here in this work, we assume the trap density is so low that the trap-assisted tunneling is ignored. This assumption is reasonable since the purpose of this work is to study the improvement of speed by incorporating of tunneling structure into injection type modulators. The ignorance of trap-assisted tunneling will over estimate R_t (degrading the speed), but it is always better to start with the worst scenario when a new device structure is proposed.

There are several device modeling approaches for tunneling structures in Sentaurus. A simple but less accurate modeling approach is to use the equivalent recombination-generation (R-G) centers to represent the tunneling process [13], [14]. Although the tunneling process is a quantum phenomenon, the net result of band-to-band tunneling is electron-hole generation and recombination. The computation complexity is substantially reduced by using R-G rate to calculate the tunneling current. The equivalent R-G rate is calculated from the tunneling carrier effective mass, barrier height and barrier width, and often requires parameter fitting from experiment data to establish an accurate model. This approach is shown effective for some specific tunneling phenomenon, such as the Hurkx model [13] for leakage current calculation in gate oxide.

A more reliable approach is to solve the Schrödinger equation by Wentzel-Kramers-Brillouin method and calculate the tunneling possibility along all viable paths across the metallurgical junction of the P^+/N^+ structure. This method employs non-local mesh tunneling model in Sentaurus. The accuracy of the numerical modeling also depends on the length of a chosen tunneling path which is defined by connecting two mesh points across the junction interface. It is known that the possibility of tunneling reduces to negligible when the tunneling path is greater than 10 nm [12], which agrees well with our numerical study of a separately modeled P^+/N^+ tunneling diode. Here in this work, we choose to use the non-local mesh tunneling model to simulate the tunneling structure and the maximum distance of tunneling path across the metallurgical junction was set to 10 nm to improve convergence. The delta-doping like profile is used in the simulation.

There is a concern of current generation due to avalanche breakdown arising from impact ionization in the reversed junction. At doping level of 10^{19} cm^{-3}, the energy bandgap of Si is 1.07 eV at room temperature considering the bandgap narrowing effect due to heavy doping [15]. For reverse junction voltage of Si device at less than 4 E_g/q ($\sim$4.4 V), quantum tunneling dominates the current [12], while between 4 and 6 E_g/q ($\sim$6.7 V), the current is combined results of avalanche and quantum tunneling. At junction voltage above 6 E_g/q, it is believed that avalanche breakdown is the dominant mechanism of junction current. In this proposed device, the voltage drop of heavily doped P^+/N^+ junction is less than 0.3 V. Thus, we believe quantum tunneling is the dominant mechanism for the current flow. However, to take into account all possible mechanisms of current flow in the reversed biased junction, we also included the impact ionization model in the TCAD simulation.

IV. Electrical Characteristics and Discussions

The device bandwidth, power consumption, size and modulation depth are all important figure of merits of a Si EO modulator for on-chip optical interconnection. The bandwidth of a modulator is affected by the *RC* time delay. The basic circuit model of an injection type modulator with tunneling structures is shown in Fig. 3(b). Resistances in a tunneling modulator include three parts: resistance of the PN junction R_j, resistance of the tunneling layers R_t, and the series resistance of the local connections and contacts R_s.

A. Resistance of the Modulator Structure

The resistance of the tunneling structures is affected by many factors including the carrier effective mass, trap density, bandgap and doping level. The tunneling current of a reverse biased junction can be calculated by multiplying the tunneling probability with the available electrons in the valence band of the P^+ layer in cell 1 and the available states in the conduction band of N^+ layer in cell 2. The tunneling possibility is obtained by integrating along all possible tunneling paths. An analytical equation for reverse current of tunneling diode is given by [16]:

$$J_t = \frac{\sqrt{2m^*}q^3\xi V}{4\pi^2\hbar^2 Eg^{0.5}} \exp\left(-\frac{4\sqrt{2m^*}Eg^{1.5}}{3q\xi\hbar}\right) \tag{4}$$

where m^* is the effective mass and E_g is the bandgap of the silicon. ξ is the electrical field and V is the applied voltage across the junction. By assuming the average electrical field is 3×10^6 V/cm in the depletion region and E_g is 1.03 eV due to degenerate doping level, the calculated tunneling current is 0.035 mA/μm under the bias voltage of -0.3 V. The current value is underestimated because silicon is dominant by indirect tunneling, which can't be well estimated by (4). A more accurate TCAD simulation using the approach described in previous part is needed to estimate the resistance of the tunneling structures.

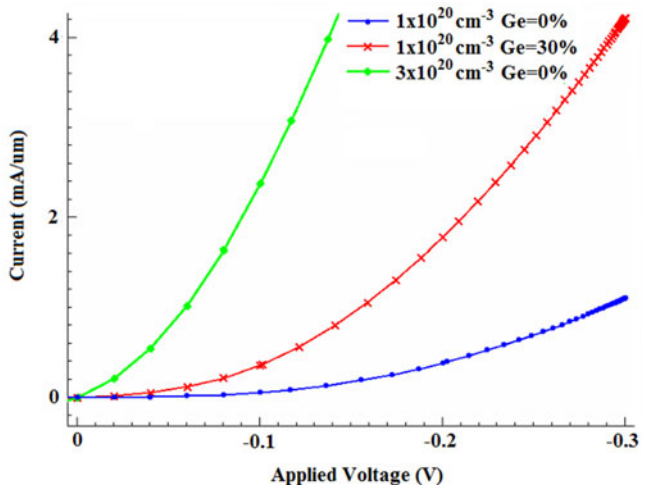

Fig. 5. *I–V* characteristics of reverse biased tunneling structure.

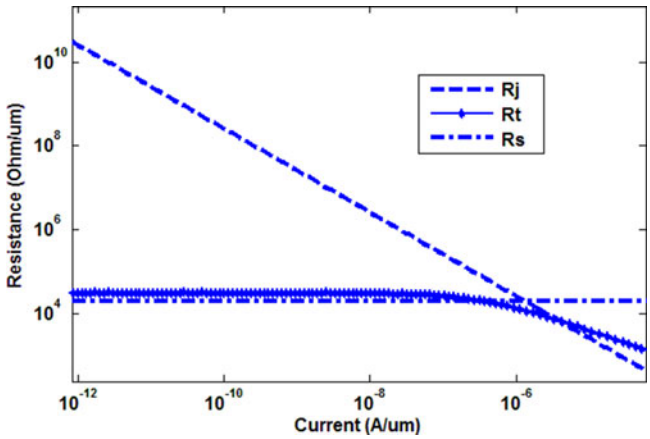

Fig. 6. Resistances in the proposed modulator: junction resistance (R_j), series resistance (R_s) and resistance from tunneling structure (R_t).

We can see from (4) that the tunneling current decreases exponentially with effective mass. To estimate the performance under the worst scenario, the electron effective mass of 0.23 m_0 and hole effective mass of 0.38 m_0 are assumed in all parts of simulations, where m_0 is the mass of free electrons. Usually the experiment extracted effective mass is slightly smaller than these standard values. Note that the trap-assisted tunneling current is excluded from the simulation. From (4), we can see that there are several approaches to reduce the resistance of the tunneling structures including increasing doping level and adding germanium composition in the silicon tunneling layer. Higher doping level leads to higher electrical filed. The incorporation of Ge atoms reduces the effective bandgap of silicon, which increases the tunneling current by lowering the barrier height. However, these two approaches also have disadvantages for the performance of an EO modulator. High dopant density gives rise to increased optical wave propagation loss while the SiGe alloy increases the fabrication complexity. These trade-offs should be considered when designing an EO modulator with tunneling structures for a specific application. A tunneling diode with an identical structure and doping (1×10^{20} cm^{-3}) as the tunneling structure in Table I was modeled separately to study the resistance of the tunneling junction. The case with increased doping levels and incorporation of 30% Ge in the tunneling layer were also studied. These results shown in Fig. 5, are consistent with our prediction. The monotonic increase of current with junction voltage indicates a nonlinear equivalent resistance of the tunneling junction. The average tunneling resistance R_t is estimated to vary from hundreds of ohms to tens of ohms for a device of 1 μm in length.

The series resistance R_s includes all resistances outside the intrinsic device region. It includes the local interconnects resistance R_L, metal contact resistance R_c, probe contact resistance and so on. The local interconnects R_L and the metal contact resistances R_c play the major role here. For a heavily doped region, the specific contact resistance is approximately 1×10^{-7} Ω·cm^2 [15]. Thus, for a contact region with size 300 nm by 1 μm, the contact resistance R_c is estimated to be 33 Ω. The distance between the heavily doped regions to the intrinsic device region is usually ~500 nm in a Si EO modulator to minimize optical loss caused by the metal contacts. This connecting region is usually moderately doped. If the thickness is assumed to be 50 nm and doping level is 1×10^{17} cm^{-3}, the calculated resistance R_L is 17.2 kΩ for the local connection region. Thus, the total series resistance can be estimated to be 20 kΩ for a 1 μm long modulator. The series resistance decreases with longer device since the current flows perpendicular to the Z direction. For a modulator with length of 400 μm, a series resistance of 20 kΩ/μm corresponds to a 50 Ω total series resistance, which is close to the measured resistance for a high speed system in practice [17].

The final part is the resistance from the PN junction, R_j. The junction resistance reduces as the current increases and can be calculated by

$$R_j = \frac{kT}{q\eta(I + I_0)} \tag{5}$$

where η is the diode ideality factor, I is the current through the junction and I_0 is the saturation current of the junction. At 0 V bias, the current is equal to the saturation current, which is calculated to be on the order of 1×10^{-15} mA/μm based on the doping level and dimensions mentioned in Table I. Assuming the ideality factor is 1, R_j is on the order of 1×10^{13} Ω/μm at 0 V bias. The junction resistance is in a reciprocal relationship with the current. With increasing current and voltage, the junction resistance decreases pretty quickly.

Fig. 6 shows how different resistances change with current. We can see that the junction resistance dominants the total resistance at low current level. When R_j drops below the series resistance R_s, the total resistance is mainly determined by the series resistance since the series resistance doesn't decrease with current. The tunneling resistance R_t doesn't dominate the total resistance at any current level.

The total resistance of the modulator configuration from Fig. 1(a) is calculated to be 22 kΩ/μm and the resistance for configuration in Fig. 4(a) is calculated to be 25 kΩ/μm at the current level of 10^{-5} mA/μm. The difference of the resistance

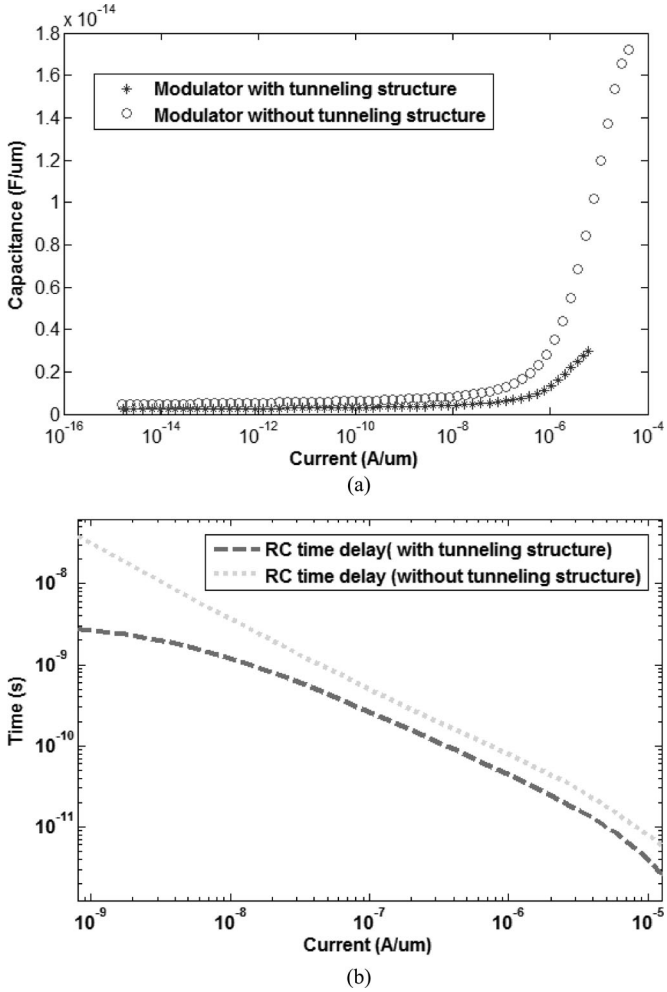

Fig. 7. (a) Capacitance of modulators with and without tunneling structure. (b) Total *RC* time delay in modulators with and without tunneling structures.

primarily comes from the tunneling structure, R_t. For a normal operation of the modulator, the current level is expected to be in the range of 0.01–0.1 mA/μm. At this current level, the tunneling resistance only slightly alters the total resistance of a Si EO modulator.

B. Capacitance of the Modulator

The capacitance was investigated by ac small signal simulations of the intrinsic device region of the modulators shown in Fig. 4(a). The doping level in the tunneling structure is set to be 1×10^{20} cm^{-3} and there is no Ge incorporation. As discussed in previous part, C_d decreases with reduced quasi-neutral region width w and is the dominant term of the total capacitance after the onset of carrier injection. We evaluated the total capacitance of the intrinsic device modulator in Fig. 4(a) (details in Table I) at different current levels. As a comparison, the total capacitance of a PiN modulator design with exact the same total dimension was also studied at the same current levels (structure is shown in Fig. 4(b)). Fig. 7(a) shows how the total capacitance of the modulator designs changes with current. A reduction of nearly half in capacitance is observed in the splitting cell

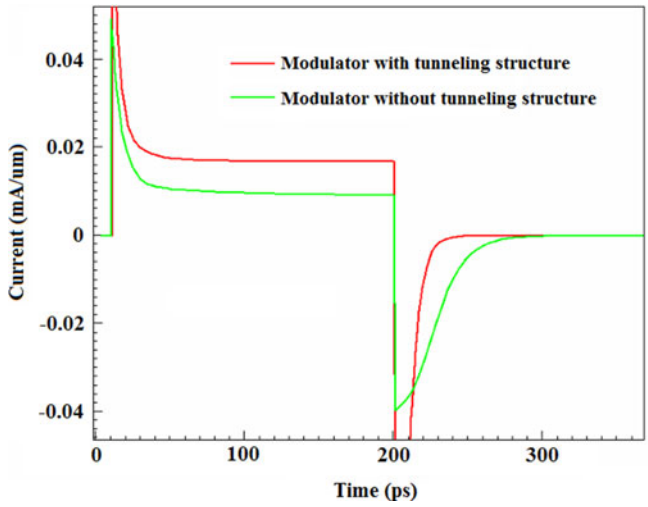

Fig. 8. Transient responses of modulators with and without tunneling structures.

modulator design. Nonlinear capacitance varying with current implies unsymmetrical impulse response of the modulator and some circuit techniques are required for the modulator driver design. The total *RC* time delay of these two modulator designs were calculated and the results are shown in Fig. 7(b).

C. Speed Response

The modulator response to a rectangular pulse signal, i.e., the transient response is a good way to verify the speed of the modulator. A transient simulation was done by applying a 2 V square wave voltage signal to the proposed modulator with tunneling structures [see Fig. 4(a)] with a rise time and fall time of 1 ps, respectively. It should be noted that only intrinsic device region was simulated and other extrinsic region was replaced by an effective series resistance of 20 kΩ/μm. For comparison, a conventional PiN modulator with the same dimension and series resistance was also simulated by applying a 1 V square wave signal. The reason for choosing 2 V signal for the proposed tunneling modulator while only 1 V for conventional PiN modulator is to ensure the current is similar. Since the proposed modulator has two PN junctions, it requires twice voltage to turn on the device. The current responses of these two structures are shown in Fig. 8. It can be seen that the current response of modulator with one tunneling structure is much faster than the one without tunneling structure.

It is well known that the relationship between the stored charge and the terminal current is quite non-linear and the current response can only give us an estimation of the speed. To get the accurate speed performance as a modulator, we need to study the carrier evolution inside the device in details because it is the carrier change that determines the optical performance. Carrier concentrations are plotted along the center of the device. Fig. 9 shows the carriers evolutions inside the device when the device is turned ON and OFF. The time step between each line in Fig. 9 is 20 ps. Rise time and fall time is defined as the time it takes carrier concentration to switch between 10% and 90%

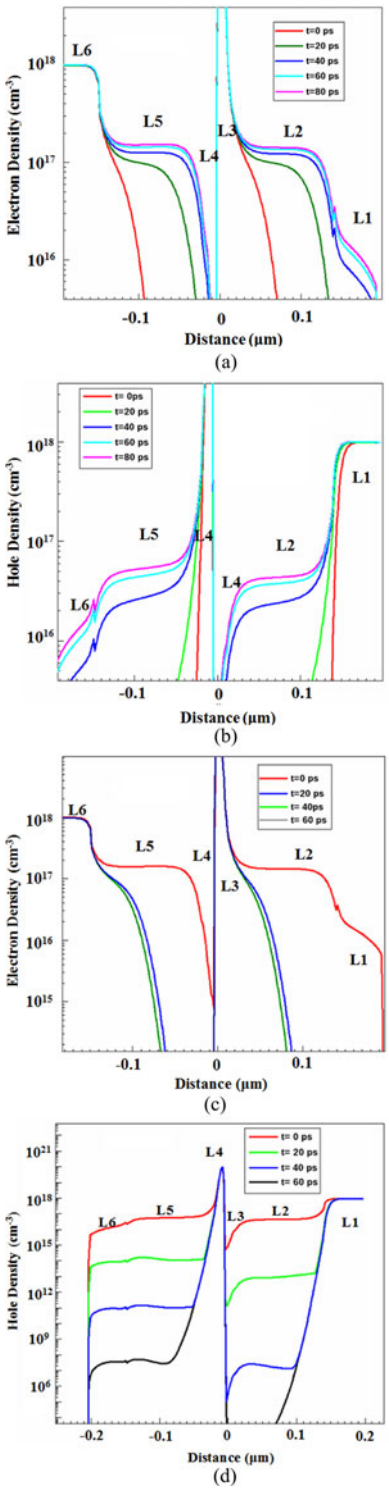

Fig. 9. (a) Electron evolution when device is turned "ON," time step = 20 ps. (b) hole evolution when device is turned "ON," time step = 20 ps. (c) Electron evolution when device is turned "OFF," time step = 20 ps. (d) Hole evolution when device is turned "OFF," time step = 20 ps.

of the dc value. The rise time for modulator with one tunneling structure is found to be approximately 70 ps and the fall time is 20 ps. And the rise time and fall time for conventional PiN modulator with the same total dimension are found to be 120 and 70 ps, respectively. Significant reduction in rise and fall time is observed in splitting cell Si EO modulator. A rough estimation of the speed of the modulator gives f $\approx 1/(t_r + t_f) = 11$ GHz.

D. Power consumption

The energy consumption is estimated based on the speed performance discussed in the above section. To transmit one bit data, the power consumption can be calculated as

$$E = 0.5 \times \int_0^{Ts} V(t) \times I(t)dt \tag{6}$$

where T_s is the period of the signal and the 0.5 pre-factor is due to the possibility of "ON" state is half for a long random non-return zero signal. The calculated energy consumption for proposed modulator with tunneling structure is 1.8 fJ/bit/μm when the signal swing is 2 V. Compared with conventional PiN modulator, the modulation voltage of the proposed modulator with tunneling structures increases by a factor of 2 due to the increased number of junctions in one modulator while the speed also improves roughly by a factor of 2. That is to say, for the integration term in (6), $V(t)$ doubles and T_s is reduced to half. Therefore, the total power consumption to transmit one bit data is roughly the same for the new structure compared with conventional PiN modulator designs. The optical configuration can adopt either Mach-Zehnder interferometer or ring resonant designs. In [4], a PiN with an estimated speed response of $\sim$1 GHz has exhibited of a bandwidth of 18 Gbps when implanted in a ring resonator structure. The splitting cell modulator design that has improved electrical bandwidth will further enhance the speed response if incorporated in a ring resonator configuration. As data rate augments, the power consumption per bit will also reduce.

E. Optical Properties

The carrier distribution from previous electrical simulation was converted to a refractive index map using an empirical equation in [18]. The refractive index map was then imported to a mode solver based on finite element method. We calculated the TE mode of the modulator and the result is shown in Fig. 10(a). The effective refractive index change of the tunneling diode modulator is $\Delta n = 0.00057$ when it is switched between 0 and 3 V. The length to achieve a π phase shift is calculated to be 1362 μm. The propagation loss for the TE mode is 130 dB/cm, which leads to a total loss of 17.7 dB for L_π length. Similar optical simulation is performed for a conventional PiN modulator design. The "ON" state of PiN has the same current level as the tunneling modulator in the simulation (0.052 mA/μm is used here). The refractive index change is 0.00048, which corresponds to an L_π of 1614 μm. The optical propagation loss is 13 dB/cm for TE mode, resulting in a total optical loss in L_π length of 2 dB. Clearly there is a trade-off between speed enhancement and optical loss with the new proposed modulator structure.

In the proposed tunneling modulator, most of the propagation loss comes from the majority carriers in heavily doped tunneling layers. As discussed in previous part, the thickness of tunneling layer is determined by the epitaxial growth capability. It should

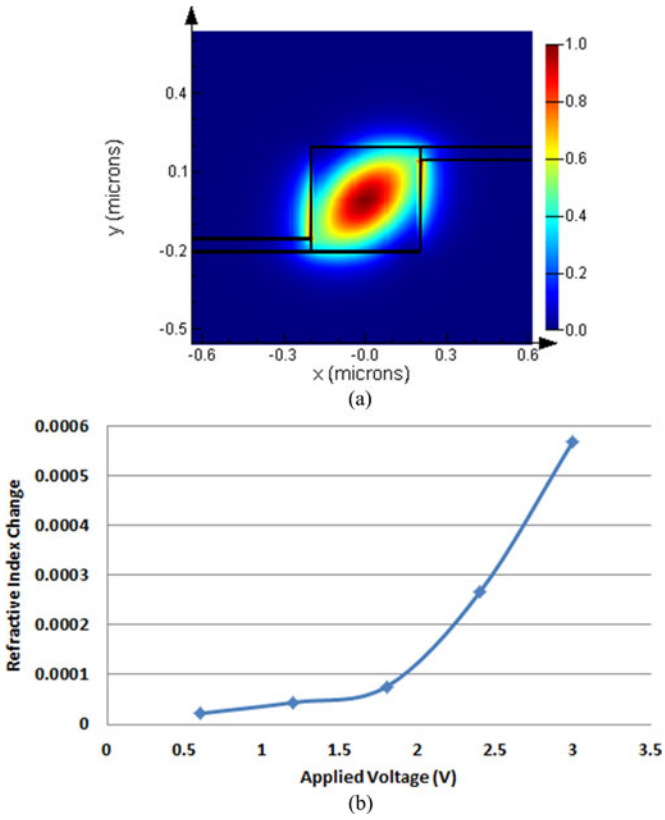

Fig. 10. (a) The calculated fundamental mode of the modulator with tunneling structure. (b) Refractive index change versus applied voltage.

be noted that the total depletion width in the P^+/N^+ tunneling junction is 6 nm under 0 V bias. In the depletion region, free carrier concentration is quite low and thus it will not introduce much optical loss. Most of the optical loss is from the remaining undepleted 7 nm thick region. If future growth technology allows the tunneling layer thickness drop from 10 to 5 nm, the undepleted region will reduce from 7 to 2 nm. By assuming the optical power distribution is uniform in the tunneling layer, the optical loss of modulator with 5 nm thick tunneling layer can be estimated by 130 dB/cm $\times$ 2/7 = 37 dB/cm, which corresponds to 4.4 dB loss for a 1 mm long modulator. Therefore, the optical loss of the proposed modulator can be greatly reduced with more advanced fabrication technology.

The change of refractive index with applied voltage is plotted in Fig. 10(b). It can be seen that the refractive index increases drastically with the increase of the forward voltage after the device is turned on. Simulation shows that the change of refractive index doubles when the signal swing is increased from 2.4 to 3 V.

V. Conclusion

The sub-wavelength confinement has become an obstacle for the continuous scaling of the silicon EO modulators, which had been the major approach to improve modulator's speed. This work explores a new method to shrink the intrinsic device size in Si EO modulators by splitting modulators into multi-cells device. Each cell is connected through tunneling structures to enable current flow. This approach scales down the dimension of the intrinsic device in the modulator but still keep the total dimension of the modulator intact. To verify the benefits, a simulation was done to study the two-cell case, where one tunneling structure is employed. The result shows that the speed is improved by a factor of 2 and the ability to alter refractive index is not degraded compared with conventional PiN modulators. The power consumption is found to be at the same level as the conventional PiN modulator. Due to heavily doped tunneling layers, the optical propagation loss increases compared with conventional PiN modulators. With more advanced fabrication technology, the thickness of tunneling layers can be further reduced for less optical loss. These results agree very well with underline principle of this approach and the speed is expected to be further improved if the modulator is split into more cells, i.e., incorporating more tunneling structures in one modulator.

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