A Mobile Test-Bed for Synchrophasor Technologies Teaching and Demonstration

Luigi Vanfretti, Emmett Williamson
Prottay M. Adhikari, Jordan Grey, Jerry W. Dziuba
ECSE Department
Rensselaer Polytechnic Institute
Troy, NY, USA
emails: {vanfrl, willie8, greyj, mondap2, dziubj}@rpi.edu

Kevin D. Jones, John D. Grimes
Jason Weaver, Tim Marshall, Matthew Gardner
Dominion Energy
Richmond, Virginia, USA
emails: {kevin.d.jones,john.d.grimes, jason.p.weaver,
tim.marshall, matthew.gardner}@dominionenergy.com

***Abstract*—This paper reports a mobile test-bed utilizing industry grade relays, phasor measurement units (PMU), phasor data concentrators (PDC), power quality meters and an antenna, for teaching and demonstrating real-time synchrophasor applications. This test-bed was accompanied with a configurable current and voltage source setup on National Instruments' compact reconfigurable input/output (cRIO) platform and a conventional PC that hosts all the software used to interface with the hardware present in the system, which can be used for demonstration and teaching of all technologies included.**

I. Introduction

A. Motivation

Over 2500 Phasor Measurement Units (PMU) are currently installed across power-stations and sub-stations in the USA. They provide the foundation of the next generation real-time monitoring America's power system. With the ability to compute and stream from 60 to 120/240 measurements per second, PMU technology is well suited for tracking power system dynamics in real-time. The motivation of this work is to construct a mobile test-bed for demonstrating PMU operations in controlled indoor laboratory environments and classroom settings.

PMUs require precise timing information for generating time-synchronized measurements. The timing information is normally acquired from GPS satellites via antennas. Thus an antenna is a key part of this proposed test-bed. Because the aim of this work is that of demonstration and teaching, it is unsafe to use real high-voltage equipment with this setup. So, for testing the setup a National Instruments' Compact Reconfigurable Input/Output (cRIO) device was used along with compatible analog output modules and dedicated electrical circuit interfaces for low-voltage signal generation. This ensures the safety of the test-bed during demonstration and teaching. In addition, the setup has industrial relays in it, it can be used for the characterization of different power system protection equipment performance at a lower cost as compared to traditional relay test-sets.

B. Related Works

Test-bed development for PMUs and their applications has been an interesting research problem for past few years. [3], [6] reported an extensive framework for PMU evaluation and bench-marking. However, [3] implementation was carried out in rated supply voltage was and not suitable for teaching in standard classroom environments due to safety requirements. On the other hand, [6] reports an extensive test-bed for evaluating PMUs (specifically for timing intrusion tests). But, this implementation is targeted towards field and laboratory environments, and not suitable for classrooms. In addition, authors in [8], [9] have developed real-time simulator based platforms for PMU and application testing, including timing intrusion [8], however, this is a cost-prohibitive approach due to the requirement of a real-time simulator. Authors in [4] proposed a cRIO based testbed for testing PMUs. But, this implementation was tested on National Instruments' proprietary PMU design only, and no industrial grade PMUs were tested using the reported test infrastructure.

This paper has different purposes and goals from that of the previously mentioned works, which is primarily teaching and demonstration of synchrophasor and related technology. To this end, and primarily for safety purposes, this papers describes how PMUs and PDCs are networked together and how they are interfaced with low voltage signals (0-5V range). In doing so, a system of PMUs and PDCs can be researched safely and cost efficiently.

The proposed test-bed, shown in Fig. 1, consists of industry-grade instruments and equipment from Schweitzer Engineering Laboratories (SEL). The equipment consists of three PMUs, one PDC, one substation clock, and one personal computer all interfaced for network connection via Ethernet switches. Additionally, a National Instruments (NI) Compact re-configurable Input/Output (CRIO) is used to drive the low-voltage input, and can be programmed to give any desired signals to the devices.

C. Contributions

The contributions of this paper are the following:

- To introduce a mobile test-bed suitable for teaching the *ins* and *outs* of different power system equipment

Fig. 1. The Proposed Test-Bed

by demonstrating their internal functions, the physical connections, and the digital communications protocols and functionalities they utilize.

- To demonstrate how the test-bed can be used to demonstrate standard functional features of power system equipment. Specifically, the test-bed is configurable for demonstrating different functionalities such as data acquisition, automation, and system protection.
- To demonstrate aspects of user-friendliness and safety in the test-bed when illustrating PMU applications in real-time. The low-voltage interface allows for signals no more than 5V, and no current driven applications which are not safe for students and teachers.

II. Components of the Test-bed

This section summarizes the equipments which were used to construct the proposed test-bed.

Satelite Synchronized Clock

The hardware contains a Satelite Synchronized Network Clock manufactured by SEL (SEL-2488). The clock works by receiving GPS signals via an SEL-9542 GNSS Antenna, and supplies the other hardwares the precise timing information.

Power Quality Meter/PMU

The SEL-735 Power Quality/Revenue meter is an industry-standard power quality evaluation equipment which is able to record and log detailed information about power quality including supply voltage, power, frequency, flicker, voltage dips and swells, voltage interruptions, transient voltages, supply voltage unbalance, voltage harmonics, rapid voltage changes, and current measurements, which are compliant with the IEC 61000-4-30 power quality standard. This particular device is also able to stream real-time synchrophasor streams (following C37.118 protocol) as outputs, thus they can function as PMUs in the context of the test-bed reported in this paper; thus allowing the test-bed for applications beyond those of PMUs.

Protection Unit/PMU

The SEL-421 protective relay has the capability of providing distance protection, under-frequency protection, breaker failure and thermal overload protection, and it can stream synchrophasor data following C37.118 protocol in real time. Thus, in the context of the current work, this relay can be utilized as a fully functional PMU unit, if desired.

Phasor Data Concentrator

The SEL-3573 PDC is capable to time-align and concentrate IEEE C37.118-compliant phasor data from multiple input synchrophasor streams. The synchrophasor inputs can be connected to this hardware via Serial link or Ethernet. If configured properly, this PDC can stream/receive up to 240 messages per second from each device.

Signal Generation Module

National Instruments' Compact Re-configurable Input/Output (cRIO) device is used to send low voltage signals to each of the PMUs. The cRIO hosts module IO cards that drive the low-voltage waveforms. In this particular implementation, an NI 9264 Analog Voltage Output Module is plugged into the first slot. The cRIO also has a Xilinx Artix-7 Field Programmable Gate Array (FPGA) and a Real-Time processor running the NI-Linux operating system on board. This device is configured, programmed, accessed, and utilized through *LabVIEW*, and is networked to the system through a standard Ethernet cable.

Network Communication

A set of network switches on the test-bed allows for each of the devices to communicate through a Local Area Network (LAN) connection as shown in Fig.2, allowing to operate the test-bench in isolation.

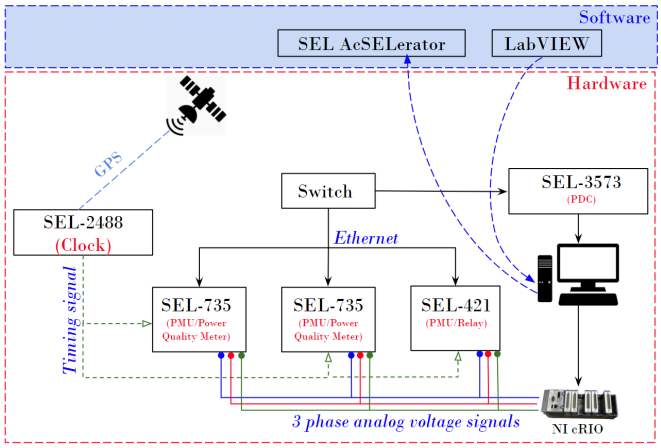

Fig. 2. Network configuration between each device on the test-bed

III. Test-bed Organization

For simplicity and context, this section is divided into three parts: hardware, software and networking. Fig. 2 shows the network configuration and physical wiring between each device on the test-bed. It also illustrates the software and hardware components of the overall setup, and demonstrates how they interact with each other.

A. Hardware

The SEL-2488 precision clock receives GPS signal through a coaxial cable from an antenna on top of the test-bed in Fig. 1). The cable is long, so that it can be placed in or outside the window of the classroom to obtain a good GPS signal. The SEL-2488 extracts precise timing information from the GPS signal and sends that information to the SEL-735 and SEL-421 devices, via IRIG-B cable. As explained in Section II, both SEL-735 and SEL-421 devices have synchrophasor functionalities and are capable of streaming PMU data in real time following C37.118 protocol. On the wooden-base of the test-bed, a cRIO-9068 hardware alongside a voltage analog output module (NI-9264) is placed and programmed to generate 3 phase voltage signals (of the range of 5V) which are fed to the SEL-735 and SEL-421 devices via breakout boards as shown in Fig. 3. Both the SEL-421 and SEL-735s have been configured for a low-voltage interface with a range of 0-6.6V peak to peak [2]. The purpose of using low-voltage interface is for the safety of the users.

The relay/PMU devices receive the low-voltage signals inside of their circuit boards and compute the synchrophasor data in real-time. Upon completion of the phasor computations, the synchrophasor data is pushed to the SEL-3573 PDC connected to the network.

Figure 3 shows the wired connections between the NI 9264 and the breakout boards that connect to each of the PMUs. Each of the PMUs are set up for a voltage input. Additionally, SEL-421 is also configured for a current input. The inputs are driven by the voltage module, so no current sources are used. It is possible to observe, measure and debug the voltage signals at this part of the circuit. One such setup is shown in Fig. 4, where a standard oscilloscope is being used to monitor the voltage signals generated by the cRIO.

B. Software

The PC that is part of the test-bed hosts NI LabVIEW which is used to monitor, configure and program the NI cRIO-9068 hardware. In principle, all the input signal generation procedure is based on this LabVIEW framework. Programs written in LabVIEW environment are generally separated into two different files. One of them runs on the on-board FPGA, and the other one runs on the cRIO chassis and utilizes the available real-time processor. The program running on the FPGA has access to the analog voltage signal generating NI-9264 module, and the program running on the chassis has access over the Ethernet/TCP network of the cRIO.

This hierarchy is demonstrated in Fig. 5(g). Each LabVIEW program consists of a front panel and a schematic (back-end). Some of the front panels designed and used in these experiments are shown in Fig. 5(a), (d) and 6(b). This part of the software-infrastructure can be construed as the *input* of the overall system.

The *output* section of this setup is monitored and configured via a collection of software packages provided by SEL. To configure the different ports of SEL-421 and SEL-735, the software package of SEL AcSELerator Architect was used. To communicate with these configured devices SEL AcSELerator Quickset software package was utilized. To connect, configure and monitor the PDC via the network, a specific software titled PDC Assistant (by SEL) was used. The data received by the PDC can be monitored in the Human Machine Interface (HMI) infrastructure from SEL AcSELerator, running on the host PC attached to the proposed test-bed. In addition, a dedicated Human Machine Interface (HMI) software for the user to view synchrophasor data and implement their own applications was built using the S3DK Toolkit for LabVIEW [10].

C. Network

The PMUs were connected to the setup via a standard network-switch and Ethernet cables, as shown in Fig.2. The computer and cRIO are also connected to the same switch.

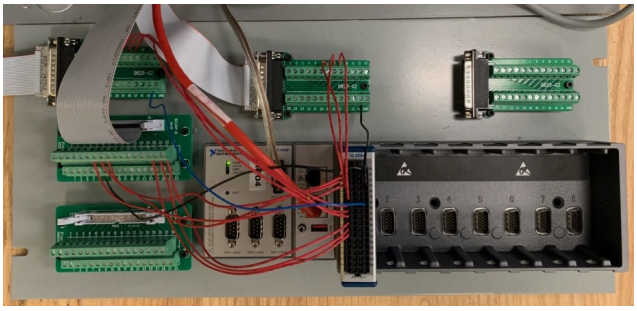

Fig. 3. Connections between the Analog Output pins of NI-9264 and the breakout board to each PMU

Fig. 4. Physical monitoring of the Voltage Outputs through an oscilloscope

IV. Case-Studies and Experiments

In order to validate the proposed test-bed, two experiments were performed. The first experiment features simple voltage/current input monitoring, and the second experiment demonstrates the over-current protection functionality of the SEL-421.

Experiment 1: Standard Input/Output Operation

As mentioned in Section III-B and demonstrated in Fig. 5(g), two LabVIEW programs are used to generate the input signals from the cRIO. One of them runs in the on-board FPGA and interact with the NI-9264 analog output module, the other one runs on the real-time operating system (host-side) of the NI-9068 chassis and interacts with the network.

The program running on the host side is used to control the voltage magnitude or current magnitude that are being sensed by the PMUs. The graphical interface designed for these controls are shown in Fig.5(a) and Fig.5(d). Ideally, according to SEL's guidelines, it is recommended to keep these voltage amplitudes below 0.44V. Since these voltages are of such low magnitude, they can be monitored physically by standard oscilloscopes without any safety concerns, as shown in Fig. 4. To prevent damage to the electronic board of the SEL equipment, the scales shown in Fig. 5(a), (d) and 6(b) impose the maximum limits that can be applied.

Once the voltage or current signals are sent to PMUs, their phasors are visible in real-time (Fig.5(a) and Fig.5(d)) by using the SEL AcSELerator Quickset's HMI monitoring functions. Since, the PMUs also stream these estimated phasor data to the PDC, they can be monitored by logging into the PDC hardware. One such real-time PDC-output is shown in Fig.5(e). It is also possible to monitor health and data-consumption rate of different incoming PMU streams from the PDC interface, as illustrated in Fig.5(f). As shown in these results, this experiment already would allow students to visualize in real-time and relate 3ϕ signals with phasors, which is an elucidating experience for students.

Experiment 2: Over-current protection

To demonstrate further functionalities beyond PMU applications, an over-current protection application is demonstrated using the SEL-421. The *Phase Overcurrent Function* feature compares the current applied to the relay to the threshold current level in the relay. This can be set in AcSELerator Quickset for any of the three phases connected to the relay. When any of the three phases exceed the over-current limit set by the user, the `TAR 50P1` bit changes from a 0 to 1. There are two ways to view when the `TAR 50P1` flag changes. The first is to use the LED screen located on the SEL-421. However, if the relay is remote, then this option is not feasible. The second option is to utilize the command terminal of the AcSELerator Quickset software, as demonstrated in Fig.6(a). The command used to monitor this is `TAR 50P1`. The parameter `67P1TC` inside the *Phase Instantaneous Overcurrent* settings is utilized to prevent the relay from operating in case the current flows in the opposite direction. It is to be noted that the *pick-up* value for the `50P1` parameter relates to the *secondary current* interpreted by the relay. The actual value of the *secondary current* is estimated by using the `CTR` parameter in the line configuration section of the *relay settings*. In this particular case, `CTR` was set to 200. Thus, for the observation in Fig.5(b), the *secondary current* is $32.62/200 = 0.16A$.

The SEL-421 is configured for a low-voltage interface, implying that all input signals are physically voltage wave forms. However, SEL-421 measures both voltages and currents on the secondaries in practice. For the overcurrent function, this transfer from voltage input to current on the secondary comes with a 1:15 scaling factor. All voltage inputs are multiplied by 15 when "measured" at the secondary. The 1:15 scaling factor is also independent from the measurements found in the AcSELerator Quickset HMI. This scaling factor must be considered when selecting the value for the `TAR 50P1 Level 1` Pickup value. To clarify, if 1A is set as the *pick-up current*, then a 66.6 mV (1/15) input (set from the LabVIEW GUI) will trigger the 50P1 bit. The GUI used for implementing the overcurrent scenario is shown in Fig.6(b), and the change in `TAR 50P1` as observed in the command terminal of SEL Quickset is illustrated in Fig. 6(a).

V. Documentation

To ensure that the test-bed can be used for teaching and demonstration, two main documents are provided to cover the hardware assembling procedures and how to use the test-bed. The first document, titled *Configuration Guide* begins with detailed explanations on how the test-bed was constructed physically. It focuses on providing information on how the Rack was constructed, and was written for the purpose of guiding undergraduate researchers or graduate students. The most important topics covered by the Configuration Guide is the process for how the low-voltage interface was built and interfaced. The *Configuration Guide* also elaborates on how each of the SEL instruments are configured, and how to set up the NI cRIO. The second document, titled the *Operational Guide* provides more information on how to use the test-bed for demonstration purposes. The *Operational Guide* focuses on providing information for students who may have to use the rack as part of a class or lab activity. The *Operational Guide* summarizes each of the SEL instruments on board, as well as how they communicate, and how to use the NI cRIO as a demonstration.

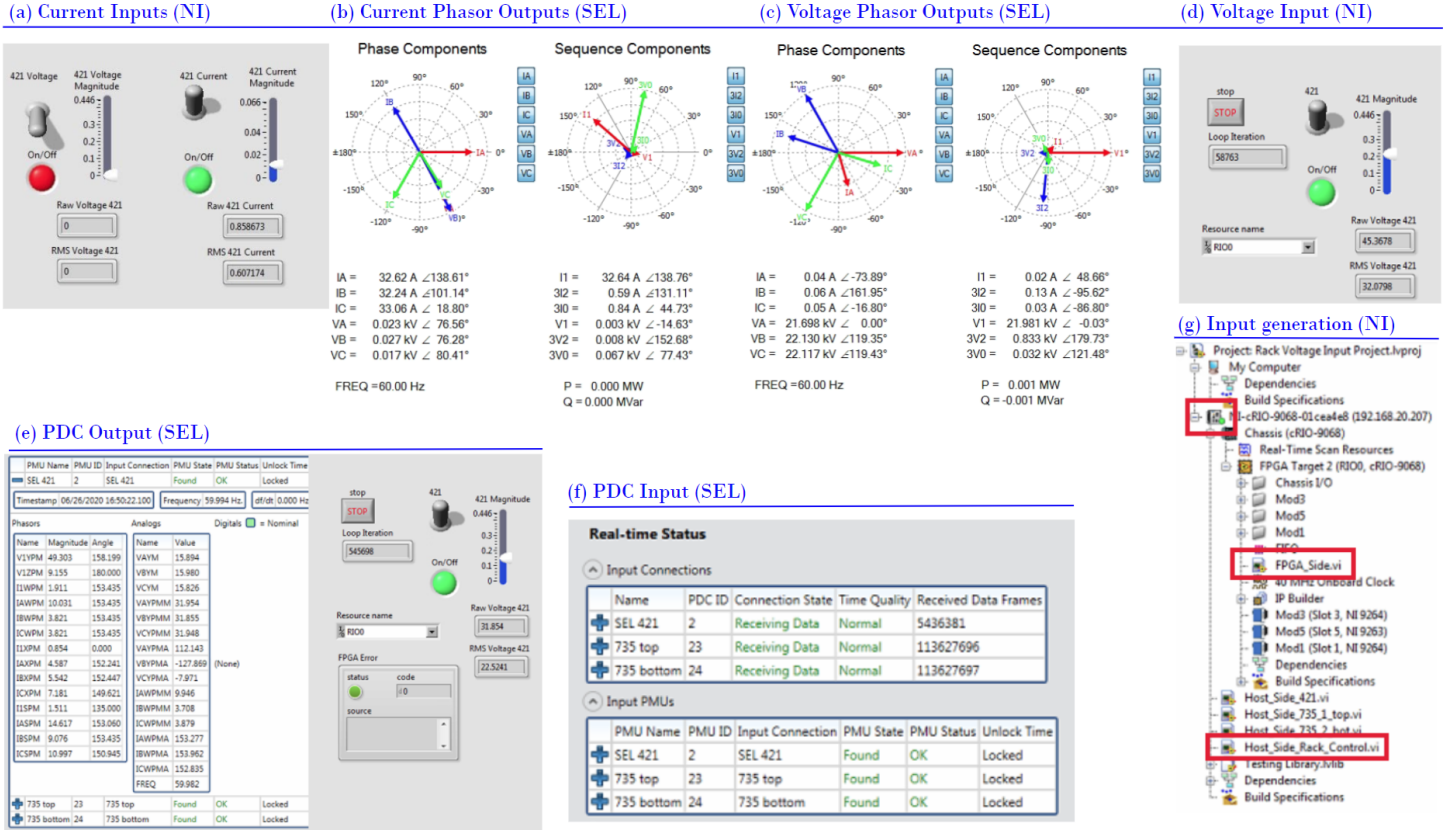

Fig. 5. Experiment 1: Input configurations and Output measurements for normal operation

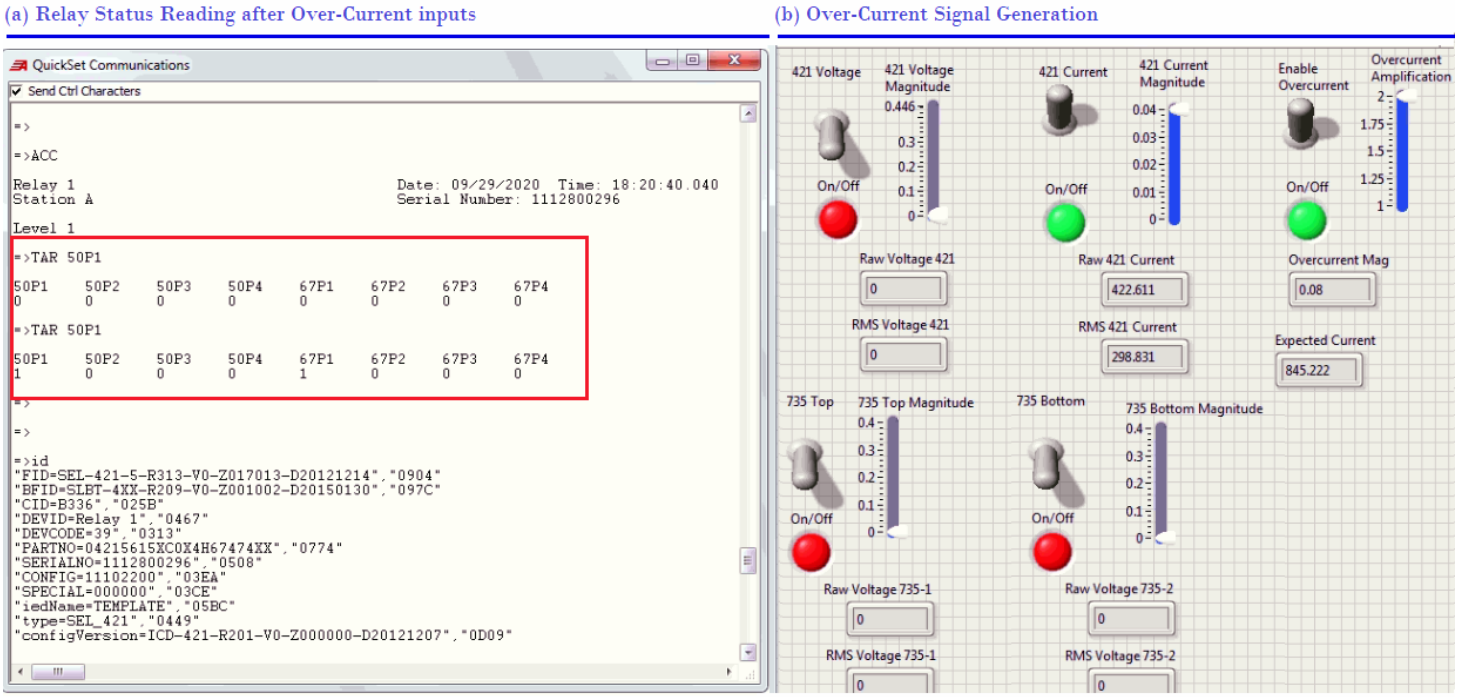

Fig. 6. Experiment 2: Demonstration of Over-current Protection

TABLE I
PROSPECTIVE EDUCATIONAL AND TRAINING ACTIVITIES SUPPORTED BY THE PROPOSED TEST-BED

Topic	HW & SW Used	Hands-On Lab. Activity	Level
Balanced/unbalanced operation	**Software:**NI LabVIEW, SEL AcSELerator **Hardware:**cRIO, SEL 421,	Demonstration of a real-time phasor representing actual analog 3 phase voltage signals	Ungergraduate
Symmetrical Components	**Software:**NI LabVIEW, SEL AcSELerator **Hardware:**cRIO, SEL 421,	Demonstration of sequence components from analog 3 phase voltage signals	Undergraduate
Protective Relaying Functions	**Software:** NI LabVIEW, SEL AcSELerator **Hardware:** SEL-421, cRIO	Demonstrating the operational region of a standard protective relay functions	Undergraduate,
PMU Data Transfer and Communications	**Software:** Wireshark, AcSELerator **Hardware:** SEL-421, SEL-3573	Introduction to C37.118.2 standards, device configuration, PDCs, networking, and analysis of data communications through the network using *Wireshark*	Graduate, Industrial
Time Synchronization	**Software:** SEL AcSELerator, SEL PDC Assistant **Hardware:** SEL-421, SEL-3573, Antenna	Demonstrating the usage of GPS signals and the accuracy of GPS timestamps, IRIB-B time distribution	Graduate, Industrial
PMU Compliance	**Software:** NI LabVIEW, SEL AcSELerator **Hardware:** SEL-421, cRIO	Demonstrating how the SEL-421 PMU performs while measuring customized voltage signals and develop PMU tests for compliance by adjusting the LabVIEW GUI	Graduate Industrial
PMU Applications	**Software:**NI LabVIEW, SEL AcSELerator, STRONgrid Lib. [10] **Hardware:**cRIO, SEL 421,	Development of simple PMU applications (e.g. real-time phase angle difference monitoring) using the STRONgrid Lib. and LabVIEW	Graduate Industrial

VI. TEACHING AND TRAINING OPPORTUNITIES

Conventional power system analysis and protection courses offered at the undergraduate level (e.g. [11], [12] and [13]) cover important concepts including phasor diagrams, balanced/unbalanced operation, symmetrical components and protection. However, they usually lack lab exposure and hands-on experiences as compared to other courses in electrical engineering. The proposed test-bed is aimed in developing new hands-on activities in teaching power systems and protection concepts. Table I demonstrates the prospective usage of this test-bed for teaching purposes, and can be used to compliment existing courses or form the basis of an entire lab course. It can be seen that, while the test-bed is useful for teaching basic undergraduate concepts like phasor diagrams, it can also be utilized to explain intricate and complex topics related to synchrophasor infrastructure, like the usage of GPS signals or the structure of C37.118 protocol. All tests would use the cRIO and the developed LabVIEW GUI, and can be safe for untrained personnel and undergrad students. This makes this test-bed particularly user-friendly, and this was the biggest motivation of using the NI cRIO in the construction of the test-bed, instead of lower-cost alternatives. The tests designed and reported in [4] can be directly implemented in the cRIO of the proposed test-bed without any major modification.

VII. CONCLUSION

This paper reported a user-friendly, mobile, real-time platform for teaching synchrophasor applications, that utilizes and incorporates multiple industry-grade equipment. The experiments presented in this paper were carried out using low-voltage interfaces, making the test-bed safe for untrained users, such as students. All the hardware and software configurations were documented for further use in various classroom/demonstration situations. Future work on this test-bed includes expanding the Operational Guide with teaching modules exploring the entire functionality of all devices, development of custom PMU applications, more advanced networking [9] and use of protection communication protocols. The long term plan is to develop curriculum for a lab-based hands-on course at the undergraduate level at RPI.

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